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Design of Multi-Rate Digital Filter for Sigma-Delta Adc in Digital Microphone

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Abstract

This project design a forth-order 24-bit Sigma-Delta Analog-to-Digital Converter (ADC) with over 130 dB Signal to Noise Ratio (SNR), which is applied to audio signal processing in the digital microphone. The digital filter adopted three-order cascade structure including CIC filter, compensating filter and Half Band filter in order to eliminate noise of the audio and reduce required the circuit area and power consumption of the sigma-delta ADC. Since CIC Filter will bring signal attenuation, this project also adopts compensating filter series with the CIC filter, which can effectively enlarge the stopband attenuation and decrease passband attenuation. In addition, this project adds the Half-band filter after the compensating filter which function is double decimation. The structure of Half Band filter is used Direct-Form Symmetric FIR to reduce the amount of operation and save the multiplication and addition operation during filtering, which significantly reduce the area of the circuit and the power consumption of the multi-rate digital filter. The experimental results show that the signal-to-noise ratio of the designed digital filter reaches 132dB, the over-sampling rate is 128, attenuation of the stopband is 157dB and the attenuation of passband is 0.0001 dB.

Keywords

Sigma-Delta ADC; Multi-Rate Digital Filter; Audio Signal Processing; CIC Filter; Compensating Filter; Half Band Filter.

1. Introduction

With the rapid development of digital integrated circuit, the signal processing system on chip becomes more and more complex. This project is based on the direction of audio processing research. Digital audio uses digital methods to record, store, edit, compress or play the sound. The front-end of the most of digital audio products requires an analog-to-digital conversion that converts analog signals into digital signals[4]. The main principle is carrying out analog-to-digital conversion of the original signal[7], then generate the digital signal for storage, and finally convert the digital signal into analog signal for playback[2].

Sigma-Delta Analog to Digital Converter is one type of over-sampling ADC. The advantage of sigma-Delta ADC is that it has a significant accuracy. The reason behind this is that its sampling frequency is much higher than Nyquist frequency, so it does not require the high anti-aliasing filtering for the input signal[3]. Through the oversampling, noise shaping and digital filtering, it reduces the difficulty of the design and achieves a high precision and low power consumption[5], which are not able to be achieved by other types of ADC, such as Nyquist ADC[8]. Sigma-delta ADC consists of two main

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

parts, which are modulator and digital decimate filter respectively[1]. The working principle is over-sampling the input signal firstly, then send this sampled signal into the digital filters for processing, and finally get the ideal signal. Digital filters in sigma-delta ADC plays the most important role in clutter removal and noise elimination.

In the 1990s, Norsworthy, Schirier and Berkeley et al. constructed single-loop 1-bit quantization, multi-loop MASH structure and single-loop multi-bit quantization sigma-Delta ADC structure in different ways, and had carried out system modeling, circuit realization and characteristic estimation for them[10]. Meanwhile, 14-bit effective accuracy ADC was achieved with the second-order single-ring structure[10].

However, the signal-to-noise ratio(SNR) of digital microphones on the market is usually below 100dB, which results in a significant reduction in audio quality[11]. In the field of IC, the development of 24-bit high-precision ADC with signal-to-noise ratio above 100dB has always been a research hotspot. Based on the implementation method and design framework of common Sigma-Delta ADC[15], this topic will complete the design of a multi-rate digital filters with SNR greater than 100dB for digital microphone based on a 24 bit sigma-delta ADC modulator. The objectives of this project are designing the combination of digital filters to compose the appropriate multi-rate digital decimation filters and carrying out the MATLAB simulation.

2. The Modulator of Sigma-Delta ADC

Sigma-delta ADC consists of two parts, which are modulator and digital decimation filters respectively[12]. The role of the modulator is sampling the audio signal and noise shaping, then convert the analog signal convert into a digital signal. This project focus on designing a appropriate multi-rate filter based on the modulator which have been designed, in order to filter out the noise outside the frequency band and reduce the quantization noise of the system[13]. Finally, it is able to further improve the SNR and make the accuracy of the ADC reach the ideal 24 bits.

This project used the fourth-order Sigma-Delta modulator, which is the interface circuit of the fourth-order capacitive micro-accelerometer. The structure of the modulator is shown below:

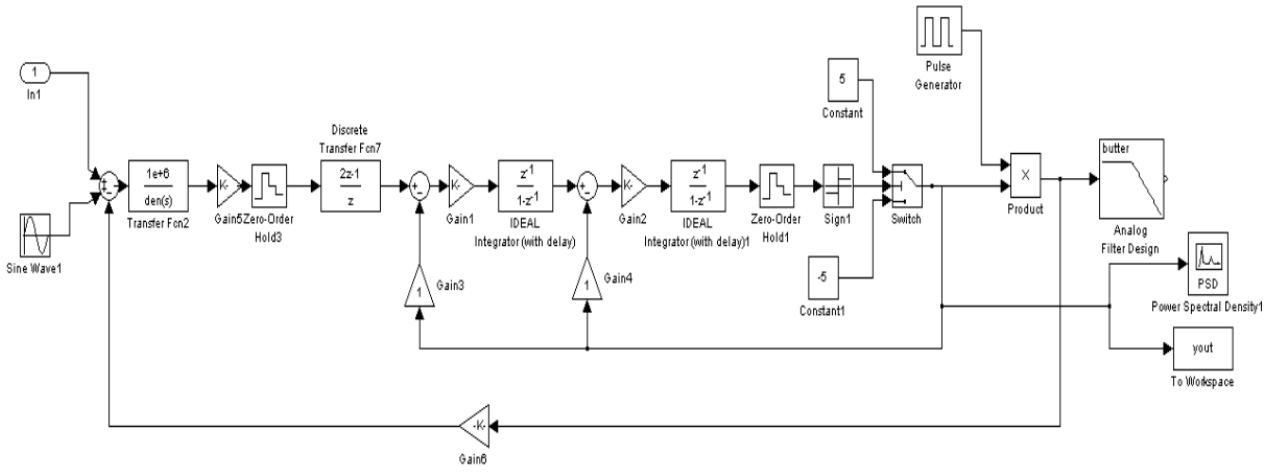

Fig. 1. The structure of fourth-order Sigma-Delta modulator

The input analog audio signal is set as 250 Hz. After processing by the modulator, it is able to output a 1-bit digital signal. The cut-off frequency is 1 kHz, the oversampling rate is 128, and the oversampling frequency of the output signal from the modulator is 2.048 MHz. The signal is then further processed by the digital filters connected behind the modulator.

After the audio signal being output from the modulator with high sampling rate, digital decimation filters are needed for the signal to experience down-sampling processing. The reduction of the

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

sampling rate not only reduces the frequency of operation per unit time, but also reduces the power consumption of the digital circuit. Moreover, the digital filters are also able to filter out the noise outside the frequency band. However, the modulator does not decrease the total energy of the noise. The noise in the signal band is transferred to the sampling frequency. Therefore the digital decimation filters are able to remove the noise in the high frequency part to improve the SNR. Finally, the digital filters also play a vital role of an anti-aliasing. Because the modulator will extract quantization noise in the frequency band, digital decimation filters need to execute the anti-aliasing processing. In conclusion, the design of digital decimation filters directly affects the SNR, power consumption, and area of the sigma-delta ADC. So it is significant to design the appropriate digital decimation filters.

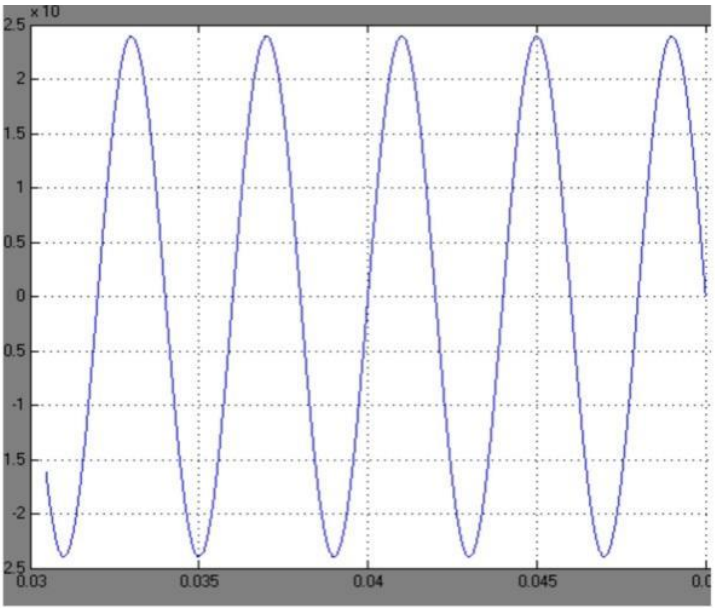

Fig. 2. The input signal with 250 Hz

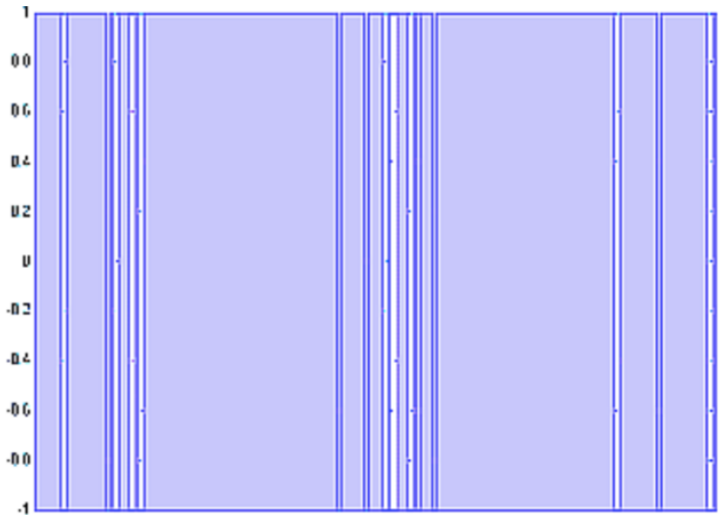

Fig. 3. The output 1-bit digital signal

3. Practical Design Procedure and MATLAB Simulation

The design of digital filters is generally divided into two categories, which are single-stage digital filter and multi-stage cascade digital filter respectively. In this project, the digital filter is constructed in multi-stage cascade in order to obtain the smaller passband attenuation of the filter, the larger stopband attenuation, and less narrow belt of transition. This project consists of CIC filter, compensating filter and Half Band filter. A diagram of the digital filter is shown below:

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

Fig. 4. The structure of multi-rate digital filter

In this structure, the first stage is CIC filter, which is used to filter high frequency signals with low resource occupancy in order to decrease the consumption. The second stage is the compensating filter, which has the function of double decimation and amplitude compensation. The third stage is the Half Band filter, which is used for double extraction with excellent performance of filtering. The multi-rate filter with this structure can effectively improve the accuracy and decrease the power consumption. The flow chart of ideal digital filter is as follows:

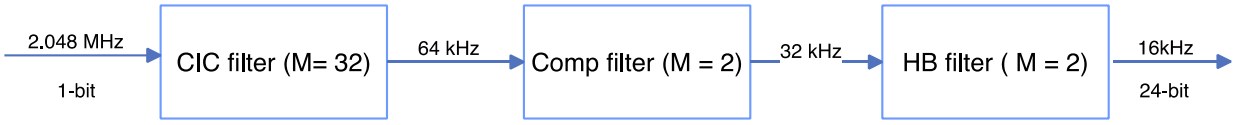

Fig. 5. The structure of ideal multi-rate digital filters

The first step of the digital filter design is to determine the structure of CIC filter. In this project, as a fourth-order modulator is designed, according to the design law of filters, the order of CIC filter K>=L+1, so the fifth-order CIC filter (K = 5) is adopted. The input signal frequency is 250Hz, the sampling frequency is 2.048 MHz, and the over-sampling rate is 128. According to the above conditions, the transfer function of the CIC filter is:

$$H(Z) = \left(\frac{1}{32}\right)\frac{1-Z^{-32}}{1-Z^{-1}} \tag{1}$$

The CIC filter designed in this project adopts the structure of Integrator + Decimator + differentiator, which used Noble identical equation that assemble the differentiator behind decimator, and the structure diagram is shown as follows:

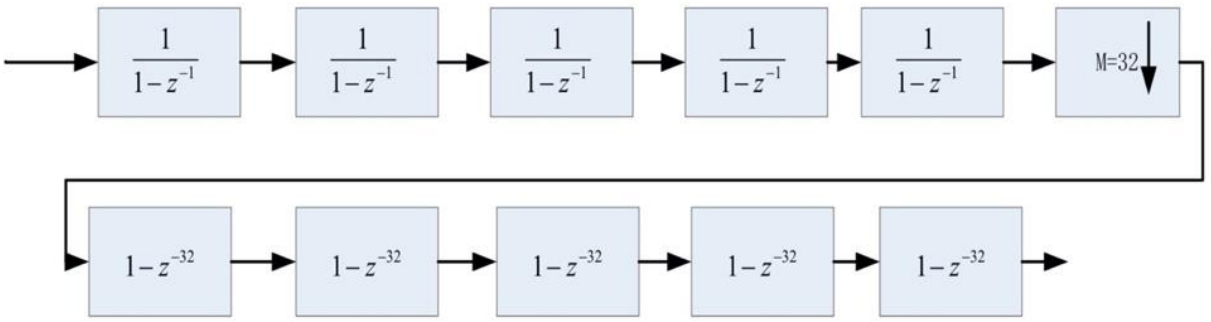

Fig. 6. The structure of CIC filter

In this structure, the signal is filtered for the first time through an integrator, then sampled down in the decimation, and finally filtered for the second time through a comb filter. In this way, the comb

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

filter will operate at the frequency which has been in down-sampling, which can effectively reduce the amount of computation in order to decrease the power consumption. The structure of CIC filter composed of specific Integrator unit and Comb filter unit is shown as Fig. 7.

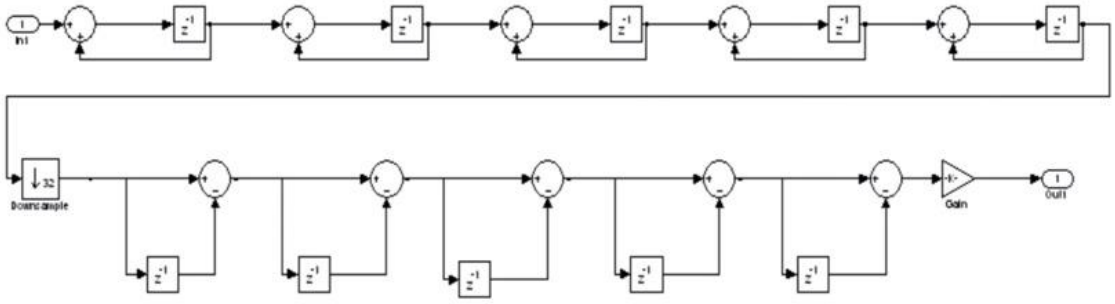

Fig. 7. The specific structure of CIC filter

The magnitude response of this fifth-order CIC filter by MATLAB simulation is shown in Fig.

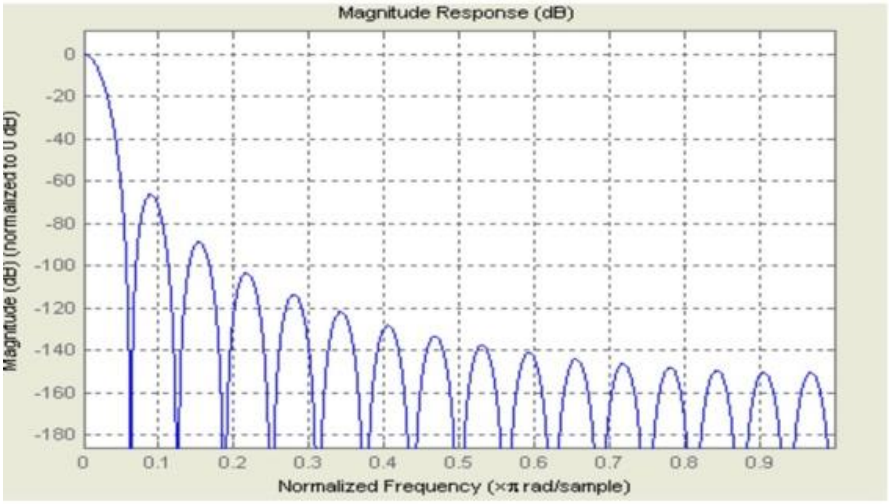

Fig. 8. The frequency spectrogram of fifth-order CIC filter (M = 32)

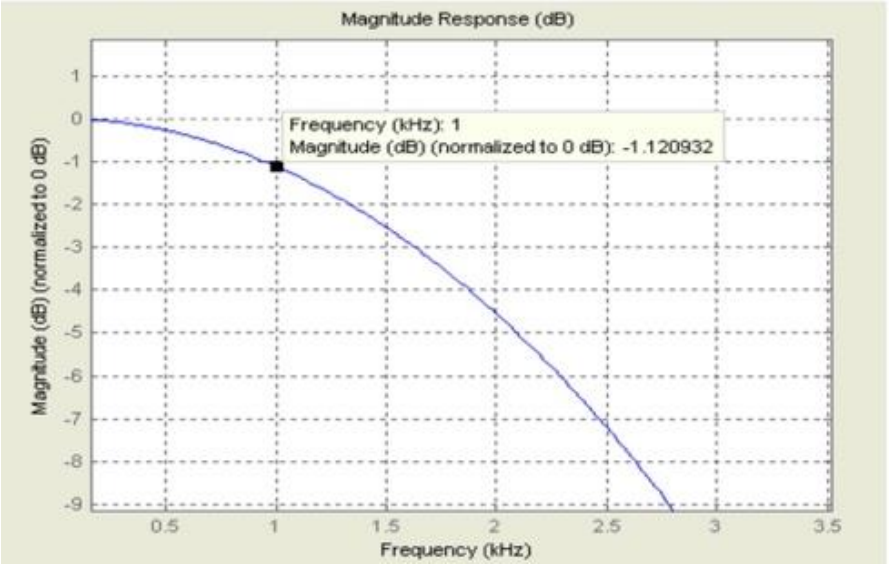

Fig. 9. The attenuation at the passband edge

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

It is necessary to check the attenuation at the passband edge of this CIC filter. The detail figure is shown in Fig. It can be observed that the attenuation at the passband edge of 1KHz is approximately 1.12dB. At this point, the signal output by the modulator is input into CIC filter for simulation, and the simulation figure obtained is shown in Fig.10.

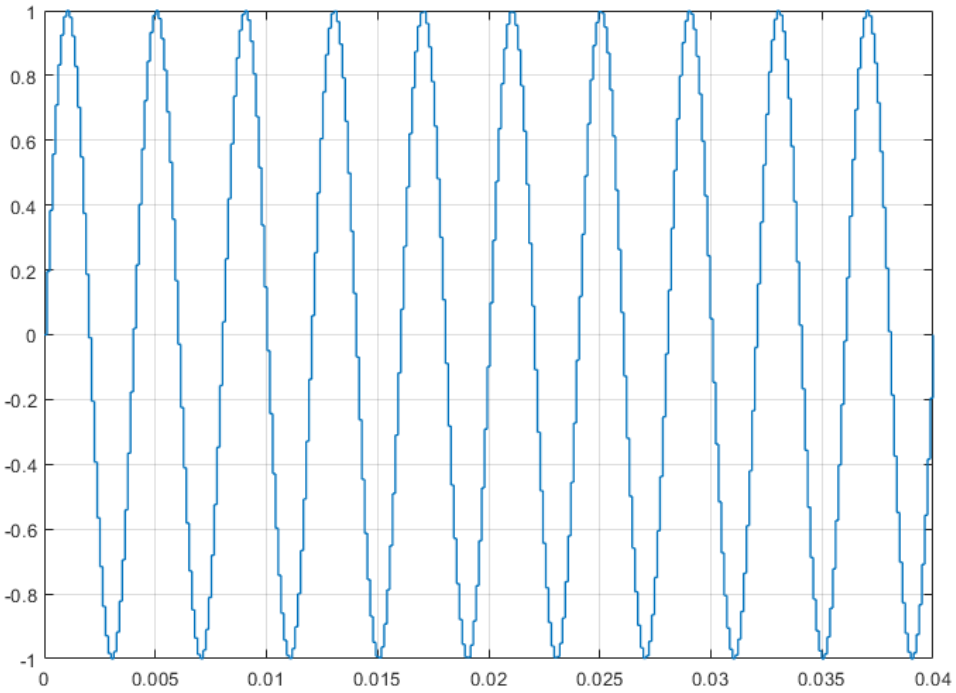

Fig. 10. The MATLAB simulation of the output signal filtered by CIC filter

According to the Fig. 10., it can be found that the output is a sinusoidal signal. The signal of each cycle is composed of 32 steps due to the decimation rate M = 32, and each step is composed of 26 significant digits. (B = 26). The length of data word (B) is determined by this formula:

$$B \geq K\, log_2(D) + Bin \tag{2}$$

In fifth-order CIC filter, K is the order of the filter which equals five (K = 5), D is the decimation rate of the CIC filter (D = 32), and Bin is the length of data word of input signal which equals one (Bin = 1). Consequently, B = 26.

As can be observed from the Fig. 10., the attenuation at the edge of the passband, there is an approximately 1.12 dB attenuation at 1KHz, which does not meet the accuracy requirements of the design of this project. Therefore, a compensating filter should be connected in series after the CIC filter to compensate the passband. Not only the function of compensation, the trimming filter also needs to double the signal decimation. After decimating 32 times by CIC filter, the sampling frequency at this time decreasing from 64 KHz to 32 KHz.

The expression of the magnitude response of the compensating filter at the passband is:

$$H\left(e^{j\omega}\right) = \frac{1}{H_{cic}\left(e^{j\omega}\right)} = \left|\frac{\sin(\omega/2)}{\sin(32\omega/2)}\right|^5 \tag{3}$$

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

Fig. 11. The magnitude response of compensating filter

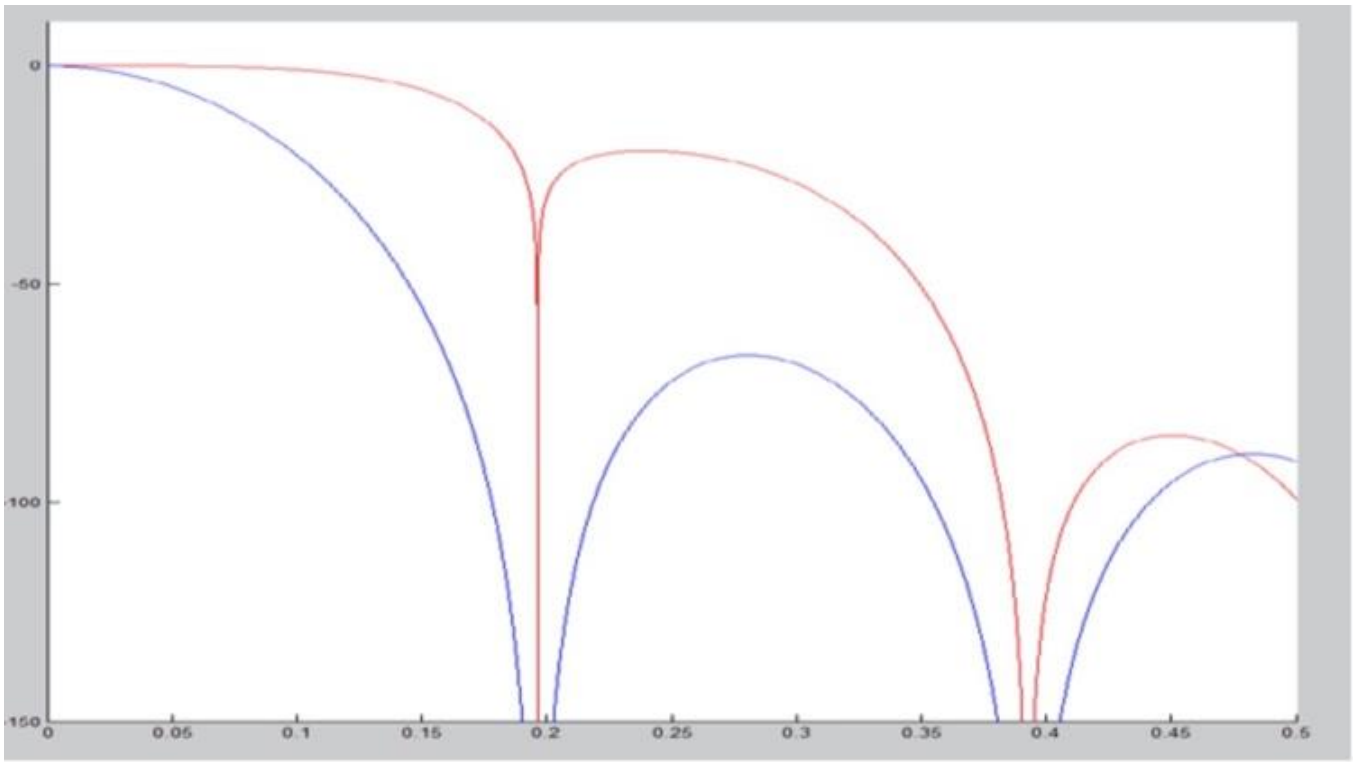

Fig. 12. The magnitude response of CIC filter and compensating filter
*Red line: Trimming filter; Blue line: CIC filter

According to Fig. 11., the compensated signal only attenuates about 0.24 dB at 1KHz.

Fig. 12 compares the magnitude response of CIC filter with the trimming filter. Through the information from the figure, it can be observed that the attenuation of passband is 0.0001 dB and the attenuation of stopband is 150 dB. After decimated 2 times by trimming filter, the output sampling

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

rate decreased from 64KHz to 32KHz, and the cut-off frequency of passband is 1 KHz. The circuit diagram was designed as symmetric form, which is shown in Fig. 13.

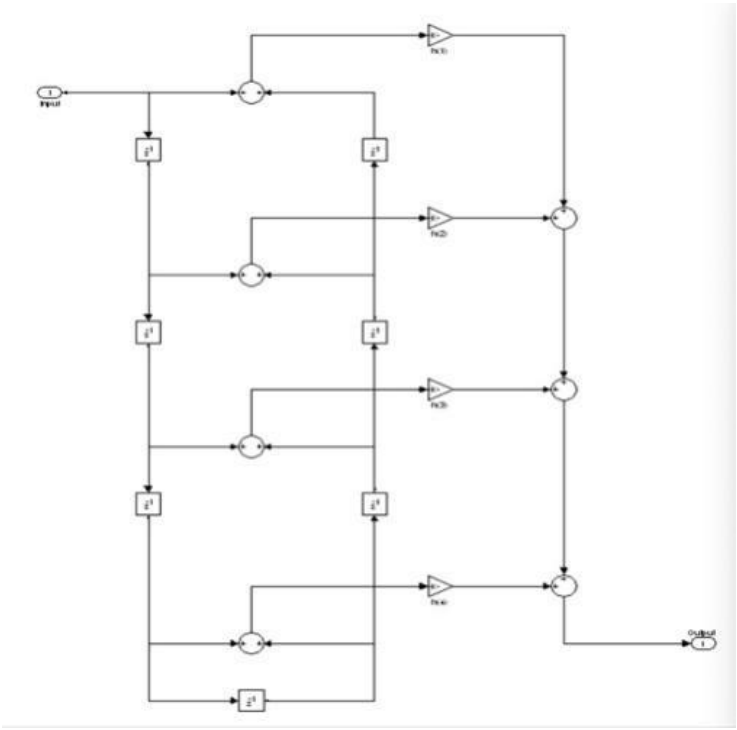

Fig. 13. The circuit diagram of compensating filter

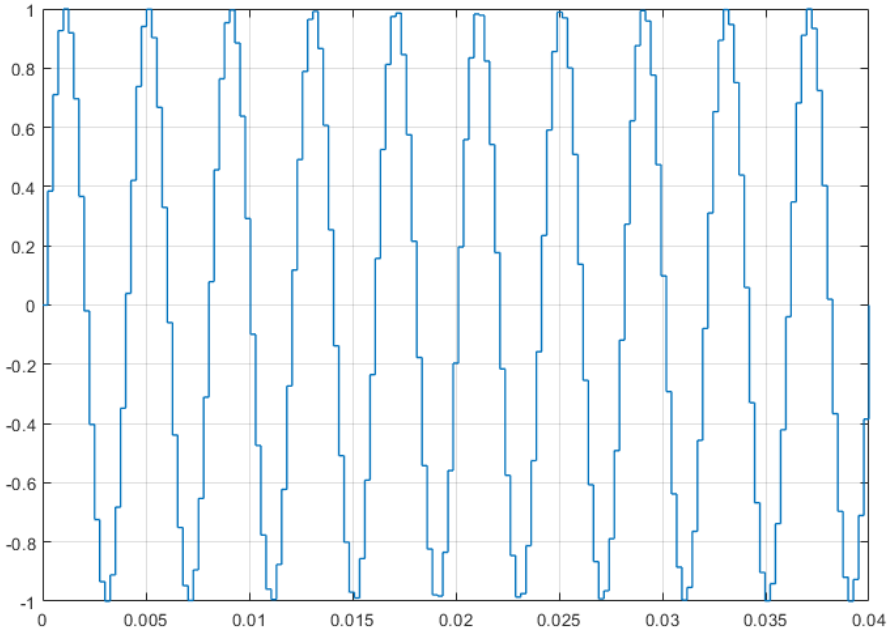

Fig. 14. MATLAB simulation of the output signal from comp filter

The output signal from the trimming filter for MATLAB simulation is shown in the Fig. 14.. According to the simulation result, after double decimation, the output signal is sinusoidal signal composed of 16 steps in each cycle. And the length of data word (B) each step remains 26-bit.

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

After the compensating filter, the sampling frequency of the signal has been decreased to 32 kHz, and the last step of down-sampling process needs to be carried out by the Half-Band filter. The Half - Band filter is designed based on the Equal-Ripple rule. By using this method, the approximate error of Half Band filter is in even distribution at the passband and the stopband in order to obtain the lower order of the filter. According to this rule, the parameters of the Half-Band filter can be determined as follows: 32 kHz sampling frequency, 1 kHz cut-off frequency, passband ripple coefficient with 10-7 dB, output signal with 24 bits, 102 orders of the Half Band filter. The magnitude response diagram of the Half-Band filter is shown in Fig. 15.

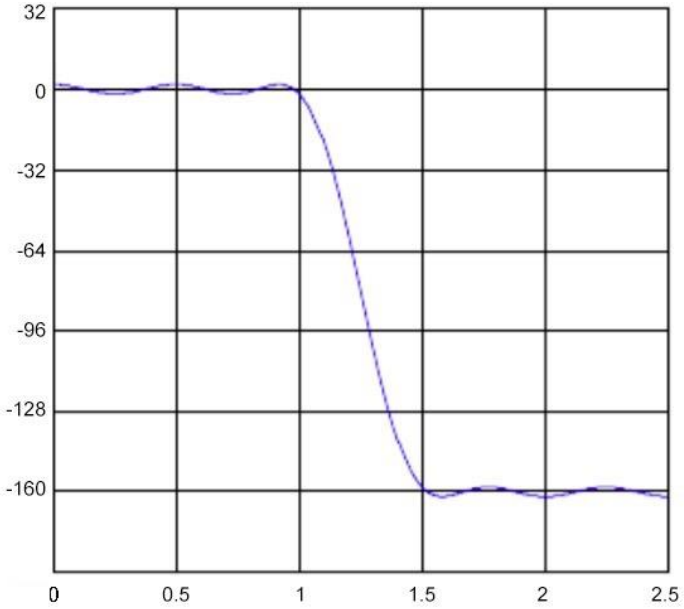

Fig. 15. The magnitude response of Half Band filter

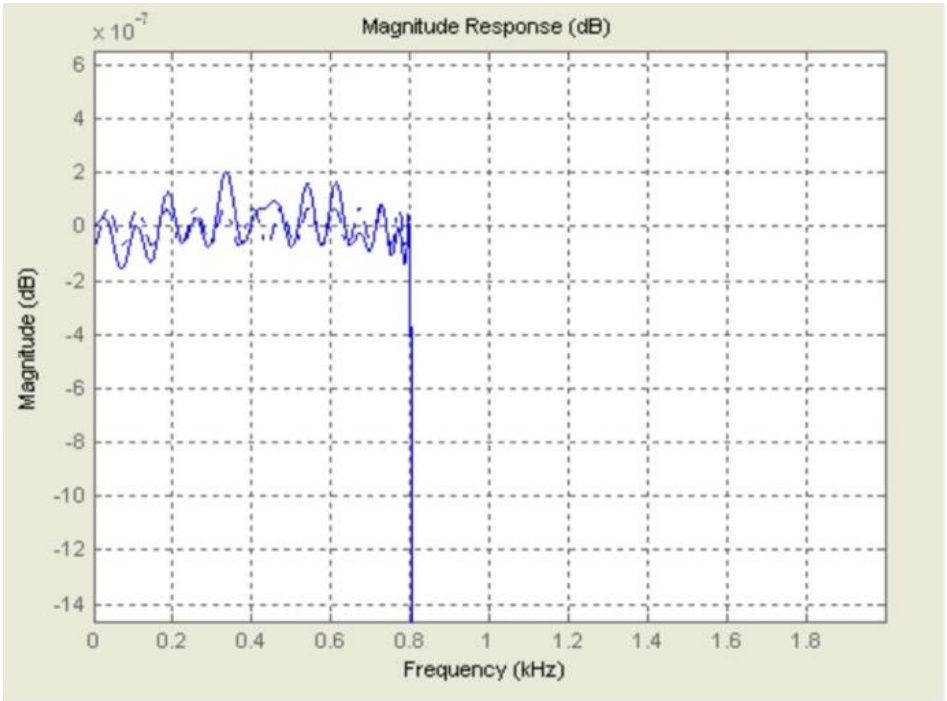

Fig. 16. The magnitude response of passband ripple coefficient

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

It can be observed that the minimum stopband attenuation of the Half-Band filter is approximately 157dB. Fig. 16. is the magnitude response of the passband ripple coefficient which is nearly 1*10-7. Half of the coefficients of the Half-Band filter are zero except for the middle term h(51). The coefficients generated by MATLAB are shown in fig. 17.

h(0)=h(102)	-0.000000070780515670776367
h(2)=h(100)	0.000000391155481338500 98
h(4)=h(98)	-0.000001423060894012451 2
h(6)=h(96)	0.000004142522811889648 4
h(8)=h(94)	-0.000010408461093902588
h(10)=h(92)	0.000023510307073593 14
h(12)=h(90)	-0.000048857182264328003
h(14)=h(88)	0.000094860792160034 18
h(16)=h(86)	-0.000173963606357574 46
h(18)=h(84)	0.000303812325000762 94
h(20)=h(82)	-0.000508457422256469 73
h(22)=h(80)	0.000819608569145202 64
h(24)=h(78)	-0.001277916133403778 1
h(26)=h(76)	0.001934342086315155
h(28)=h(74)	-0.002851914614439010 6
h(30)=h(72)	0.004108455032110214 2
h(32)=h(70)	-0.005801368504762649 5
h(34)=h(68)	0.008056886494159698 5
h(36)=h(66)	-0.011048331856727 6
h(38)=h(64)	0.015033744275569916
h(40)=h(62)	-0.020437635481357574
h(42)=h(60)	0.028045382350683212
h(44)=h(58)	-0.039534486830234528
h(46)=h(56)	0.059283807873725891
h(48)=h(54)	-0.1034199483692646
h(50)=h(52)	0.317405838519334 79
h(51)	0.5

Fig. 17. The coefficient of the Half Band filter calculated by MATLAB

Since FPGA is not able to recognize the floating point values generated by MATLAB, these floating point values need to be converted to fixed-point values for FPGA verification. Quantization of Q method is used in this project, which is to multiply the coefficient h(n) by 2Q. Q equals 15, then convert all the coefficients into binary numbers. Consequently, the fixed-point coefficients can be expressed as:

$$h(N) = h(n) * 2^{15} \tag{4}$$

This project finally adopts the class of symmetry structure to design the Half-Band filter. The circuit diagram of the Half-Band filter is shown in Fig. 18.

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

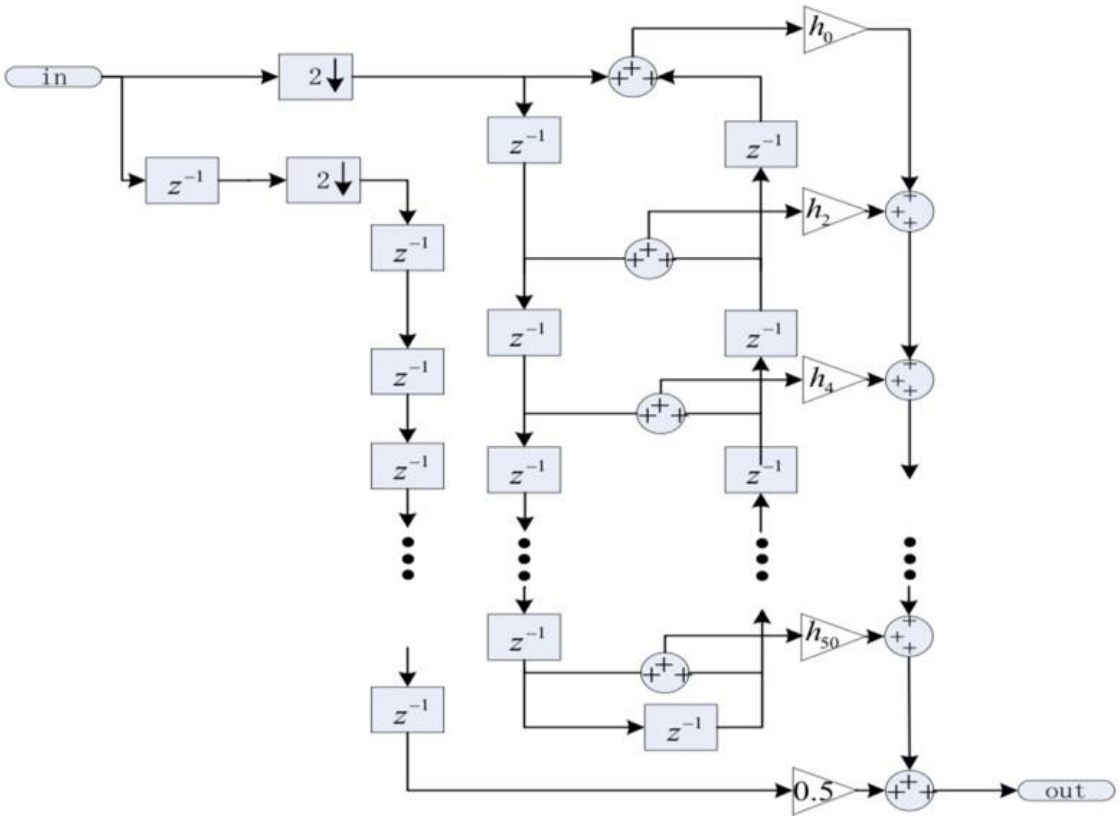

Fig. 18. The circuit diagram of Half-Band filter

Finally, the signal from the compensation filter is input into the Half-Band filter, and the output signal obtained by MATLAB simulation is shown in Fig. 19.

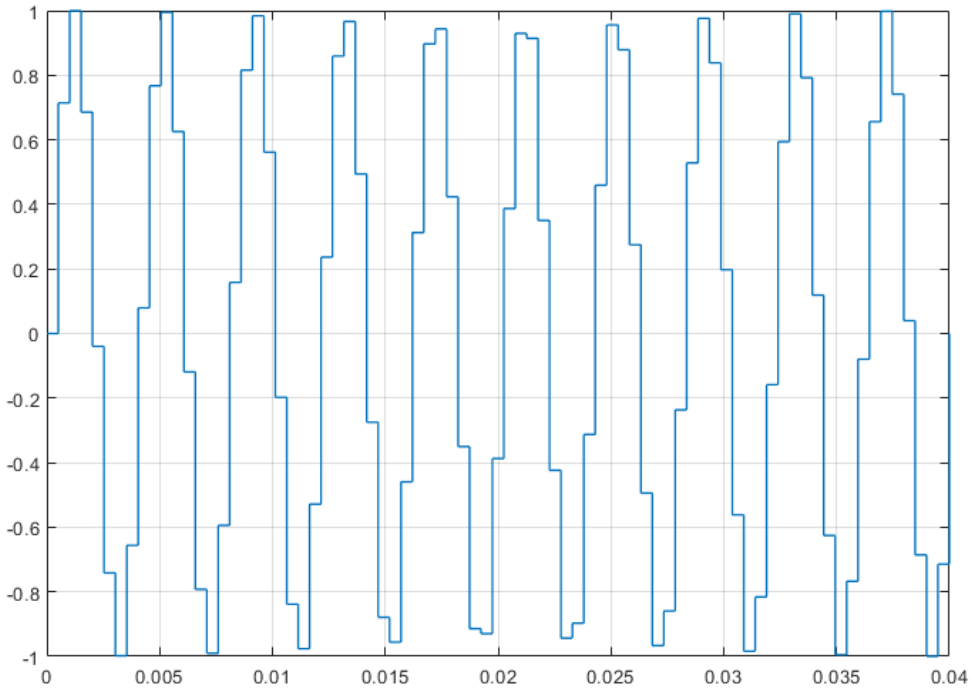

Fig. 19. The MATLAB simulation of the output signal from the Half Band filter

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

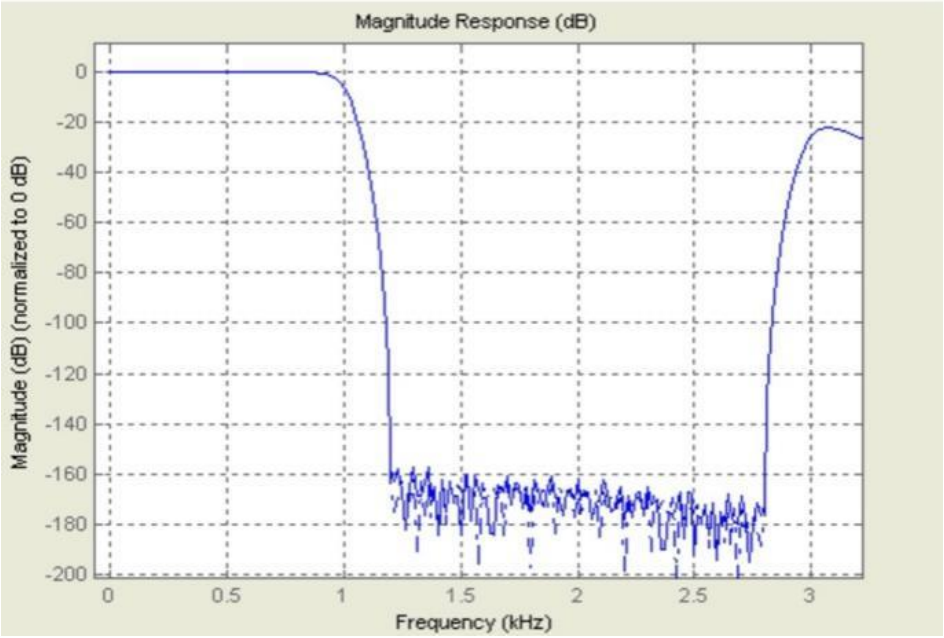

Fig. 20. The magnitude response of three-order cascade digital filter

It can be clearly observed from the figure that the final output signal is a sinusoidal signal composed of 8 steps in each cycle, and the length or data word of each step decreases from 26-bit to 24 bit, thus obtaining the final output signal of the whole multi-rate digital filter. Fig. 20 is the magnitude response of this three-order cascade digital filter.

According to the information in the Fig. 20, the minimum system attenuation of stopband is approximately 157 dB and passband ripple is about 0.0001 dB, which meet the accuracy of the design requirements. Meanwhile, due to the limitation of the digit length of the Half Band filter coefficient, CSD coding method is adopted to intercept the coefficient in this project.

SNR is the ratio of useful signal power to noise power. This project is a design of 24-bit accuracy digital filter, the ideal SNR should reach about 150dB. However, the difference between the ideal model and the actual circuit is inevitable. Fig. 21. And Fig. 22. present comparison between the SNR of the output signal from the modulator with that from the multi-rate filter.

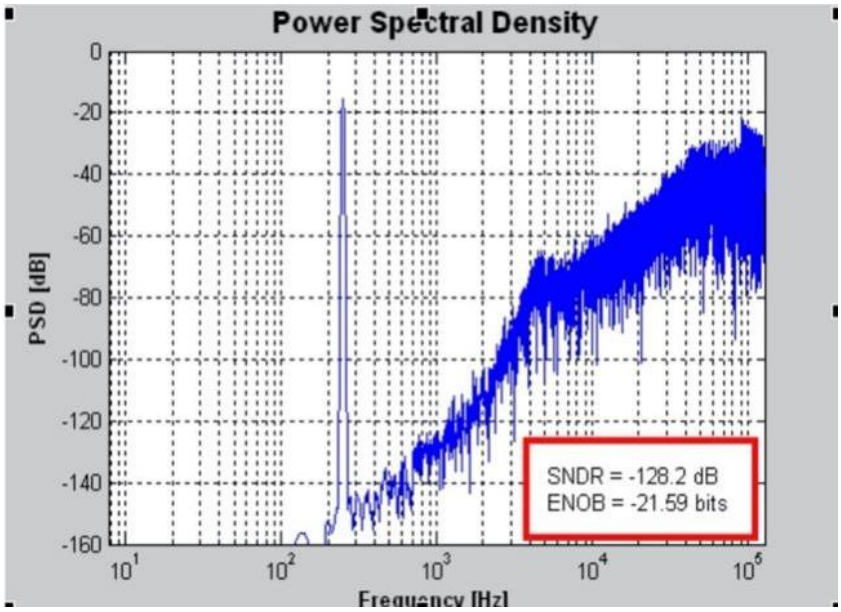

Fig. 21. The power spectral density of the modulator signal.

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

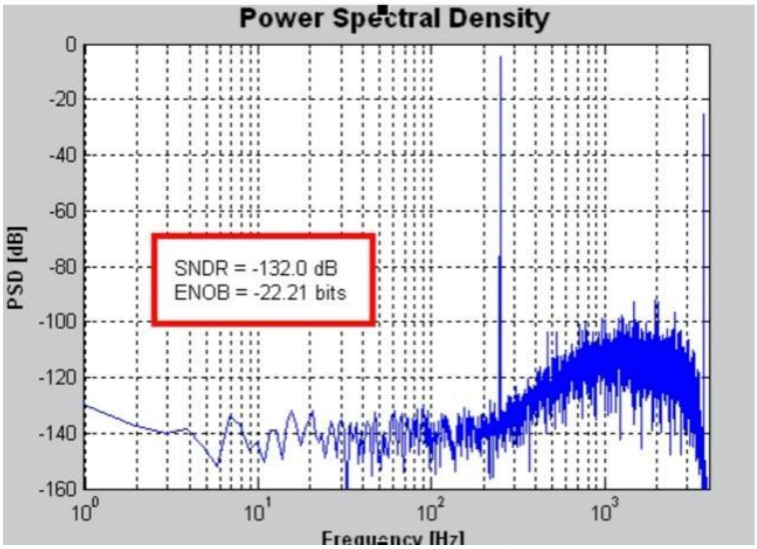

Fig. 22. The power spectral density of the multi-rate filter signal

According to this comparison, the SNR of the signal output from the modulator is only 128.2 dB. However, after the signal passing through the multi-rate filter, the SNR reaches 132 dB. Consequently, the multi-rate digital filter plays a good noise filtering function, which significantly improve the signal-to-noise ratio.

In conclusion, the design of digital filters based on sigma-Delta ADC has already been accomplish. According to the MATLAB simulation, the accuracy of the multi-rate filter is 24 bits, the sampling rate is 128, the cut-off frequency is 1KHz, and the SNR is 132 dB, which indicates that the digital filter performs a good noise filtering function in order to raise the SNR, and reduce the sampling frequency, which effectively reduce the power consumption of the system.

Table 1. The comparison between this project and other digital microphone

Reference	This project	[1]	[2]	[3]	[4]	[5]
D (bits)	24	16.79	18	16	14.87	13.15
SNR(dB)	132	102.8	110	87.2	103	98
Structure of modulator	4-order	4-order	4-order	2-order	4-order	2-order
Over-sampling rate	128	64	64	64	128	64

It can be seen that compared with the multi-rate filter in the existing products of digital microphone, this design achieves higher SNR on the basis of maintaining high precision.

4. Conclusion

In today's audio signal processing field, signal-to-noise ratio, over-sampling rate and the accuracy are the important parameters to measure the quality of digital filter. Sigma-delta A/D converter can achieve relatively high precision with relatively simple circuit, and it is widely used in high-resolution and high-precision converters. The converter is composed of analog modulator and digital decimation filter. The analog modulator can effectively reduce the quantization sound in the signal bandwidth and move the noise outside the signal bandwidth by using oversampling technology and noise shaping technology. The digital decimation filter can filter the out of band noise.

ISSN: 2414-1895 DOI: 10.6919/ICJE.202202_8(2).0092

In this project, the combined structure of three-order cascade with CIC filter + compensating filter + Half Band filter is adopted. Since CIC filter has some disadvantages, we add a trimming filter to compensate it, that is to implement the compensation of passband attenuation and in order to reduce the computational complexity.

The filter design at all levels is implemented based on MATLAB FDA toolbox, and the model is established. The output signal of the modulator is the input signal of the digital filter, which is a 1-bit digital signal with the frequency of 250 Hz, a sampling frequency of 2.048 MHz. Then the modeling and Simulation of modulator and filter are implemented in Simulink. Finally, the 24-bit 16 kHz sampling frequency digital signal is obtained, the signal-to-noise ratio is 132 dB, the minimum attenuation of stopband is 157 dB, the passband ripple is 0.001 dB, and the over-sampling rate is 128, which meets our design requirements. In conclusion, based on the current market demand and research status and design principle, this project designed an audio processing digital filter with high performance.

However, this design is only a phased research result, and can be improved in the two aspects. Firstly, there is still room for improvement for higher SNR, higher sampling magnification and higher resolution. Secondly, this design adopts the design of five-order CIC filter, 11-order compensating filter and 102-order Half Band filter. The large filter order will also affect the computation of digital filter which results in the lager audio chip area and power consumption. Therefore, it is necessary to consider how to decrease the order of the CIC filter, compensating filter and Half Band filter in order to obtain the lower power consumption and smaller chip area.

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