

Design of Programmable Signal Generator

Peng Zhang, Haoran Li, Yuhang Li

College of information science and technology (College of network security, Oxford Brooks College), Chengdu University of Technology, Chengdu, 610059, China.

Abstract

This article aims to design a programmable function signal generator based on AT89C52, AD9833 and AD8051. The programmable signal generator can realize the generation of triangle wave, rectangular wave (including square wave) and sine wave, and the frequency, amplitude and duty cycle can be adjusted separately. The AD9833 waveform generator is controlled by the AT89C52 single-chip microcomputer to generate triangle waves, rectangular waves (including square waves), and sine waves. After the potential is adjusted by a digital potentiometer, the signal is amplified and output by the high-speed operational amplifier AD8051. The frequency of the output signal is controlled by the current at the oscillation frequency reference current input terminal, the voltage at the oscillation frequency reference current input terminal, and the external capacitance at the external oscillation capacitor terminal. The duty cycle is controlled by the pulse duty cycle adjustment input terminal voltage control, and the output signal The amplitude is adjusted and controlled by the digital potentiometer MCP41010. The test results found that three kinds of waveforms-sine wave, triangle wave, and square wave can be freely converted through the button control, and the amplitude and frequency of the output waveform can be increased or decreased sequentially through the button. Within the frequency range of 10MHZ, three output waveforms The signal is in good condition and there is no obvious distortion. Through the later physical test process, it is found that the design of the programmable signal generator has the advantages of low delay, low loss, high integration and strong anti-interference ability. Complete the generation and test tasks of program-controlled signals.

Keywords

Programmable Signal Generator; AD9833 Waveform Generator; High-speed Operational Amplifier; Digital Potentiometer MCP41010.

1. Introduction

With the rapid development of electronic technology, program-controlled signal generators play an important role in communication, measurement, scientific research or teaching [1]. For example, the programmable signal generator has a very wide range of important uses in the circuit design experiment related to communication and measurement and the detection of signal equipment; and with the rapid development of electronic science and technology, the design ideas for various functional programmable signal generators And the programs have become diverse, and the design technology has become more advanced and complete. In today's era of economic and technological development, there are higher requirements for corresponding test instruments and test methods. Program-controlled signal generators have become a vital part of test instruments [2]. Therefore, the development of a high-precision, low-power and high-speed programmable signal generator is of great significance.

2. System overall scheme

The programmable signal generator can generate three kinds of waveforms, triangle wave, rectangular wave (including square wave) and sine wave, and the frequency, amplitude and duty cycle can be adjusted separately [3]. It is based on a DDS chip, the AD9833 waveform generator, to complete its waveform generation design. The main control chip adopts the AT89C52 single-chip microcomputer. The two are connected through three ports to realize data transmission, clock control and DDS working state control [4]. The biggest feature of the program control signal generator is that the AT89C52 single-chip microcomputer controls the AD9833 through the SPI interface to generate sine waves, triangle waves and square waves of different frequencies [5]; the output waveform signal frequency refers to the current, voltage and external oscillation of the input terminal through the oscillation frequency. The external capacitance of the capacitor is jointly controlled; the duty cycle is controlled by the pulse adjustment input voltage duty cycle; the output signal amplitude is controlled by the digital potentiometer MCP41010 for potential adjustment, and finally the output waveform signal is controlled by the signal amplifier AD8051 Amplify the signal accordingly. The overall program structure diagram of the programmable signal generator is shown in Figure 1.

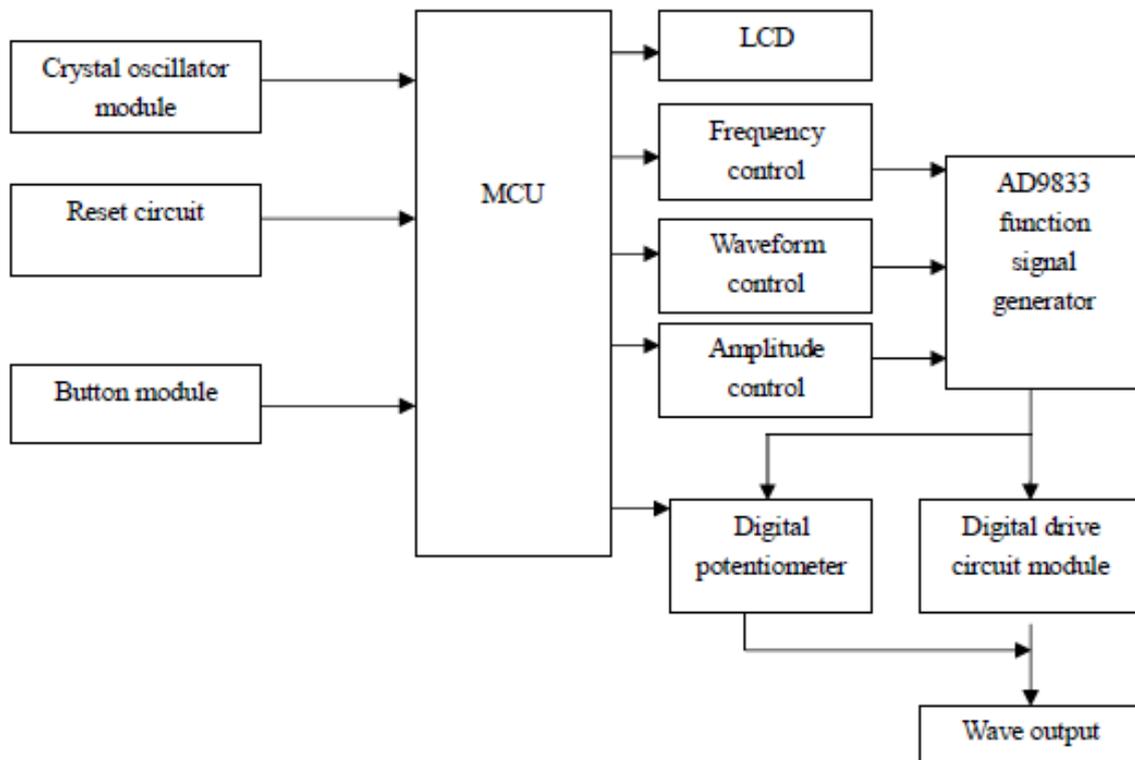


Figure 1. Structure diagram of the overall scheme of the programmable signal generator

3. Unit circuit design

The program-controlled signal generator mainly includes large modules: single-chip main control module, DDS module [6], digital potential adjustment module; the single-chip main control module controls the waveform generator module through the SPI interface to generate three kinds of waveforms-triangle wave, rectangular wave (including square wave)) And sine wave; the generated waveform data is effectively displayed through the LCD module for easy observation.

3.1 Design of the single-chip main control module

AT89C52 is a low-voltage, high-performance CMOS 8-bit microprocessor with 8K bytes of flashing programmable and erasable read-only memory, commonly known as single-chip microcomputer [7].

The electrical erasing of the entire PEROM array and the three lock bits can be completed by the correct combination of control signals and keeping the ALE pin at a low level for 10ms. The XIAL1 and XIAL2 interfaces of the single-chip microcomputer are respectively connected to a 30PF capacitor, and a 12MHz high-stability, passive crystal oscillator is connected in the middle. It forms a fixed-frequency oscillator with the inverting amplifier in the AT89C52 to provide a stable clock signal to the CPU. The reset operation has three modes: automatic power-on reset, button level reset and external pulse reset. This design uses the button level reset mode. Among them, XTAL1: the input of the reverse oscillator amplifier and the input of the internal clock working circuit; XTAL2: the output from the reverse oscillator; RST: reset input. When the oscillator resets the device, keep the RST pin high for two machine cycles. The main control module diagram of this one-chip computer is shown as in Fig. 2.

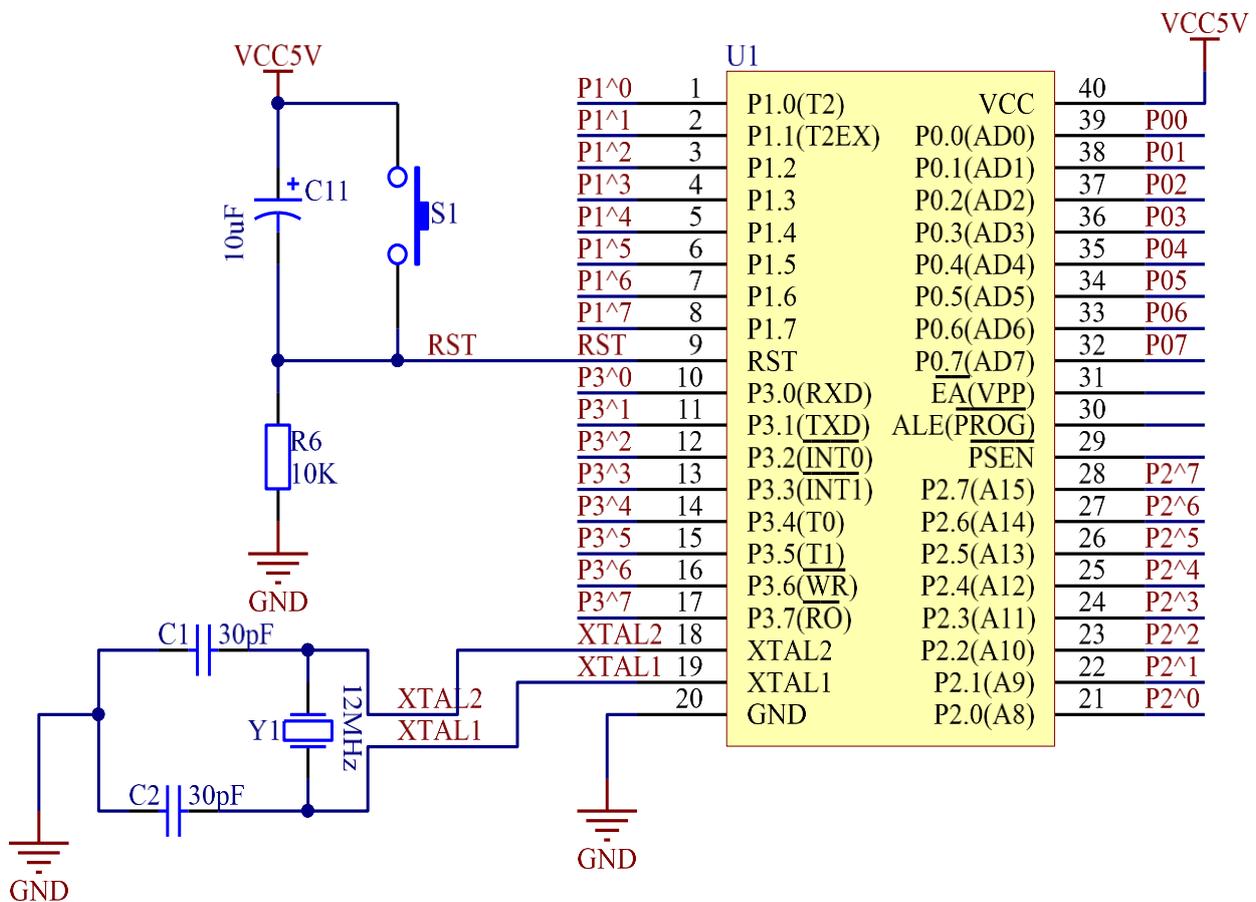


Figure 2. Main control module diagram

3.2 Selection and design of digital potentiometer

MCP41010 is an integrated digital potentiometer produced by Microchip Company [8]. It integrates a 10K digital potentiometer on a single chip. The sliding end of the potentiometer has a total of 256 discrete adjustment nodes, and there is an 8 b E2PROM data register, which directly controls the position of the sliding end on the potentiometer. MCP41010 is available in an 8-pin dual in-line package. Among them, PW0 is the potentiometer sliding end; PA0 and PB0 are the two terminals of the potentiometer; SCK and SI are the serial clock and serial data line of the SPI bus.

The internal structure of MCP41010 is shown in Figure 3. As can be seen from Figure 3, this chip contains: SPI bus interface and a POT (potentiometer). There is an 8b sliding brush control data register in the POT. MCP41010 has an SPI bus interface and uses a simple 2 B command structure.

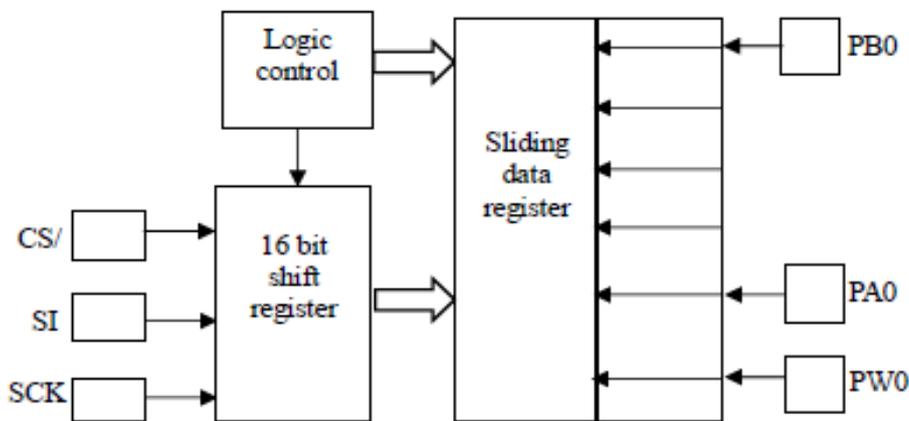


Figure 3. MCP41010 internal structure diagram

The instruction of MCP41010 consists of two sections, each section has a byte: the first section is the command byte, and the second section is the data. The schematic diagram of instruction sequence transmission of MCP41010 is shown in Figure 4. Write the command byte first and then the data byte. CS is the digital potentiometer chip selection terminal. Only when CS is low, the command word and data word can enter the 16-bit shift register. When the rising edge of CS occurs, the value of the shift register enters the data register, thereby changing the resistance value of the potentiometer. SCK is the clock line, and data enters the SI data line on the rising edge of SCK. The device will automatically monitor the number of pulses of SCK when CS is low at the rising edge of CS, that is, the number of rising edges. The command can only be executed when the clock number is a multiple of 16, otherwise the command will be invalid.

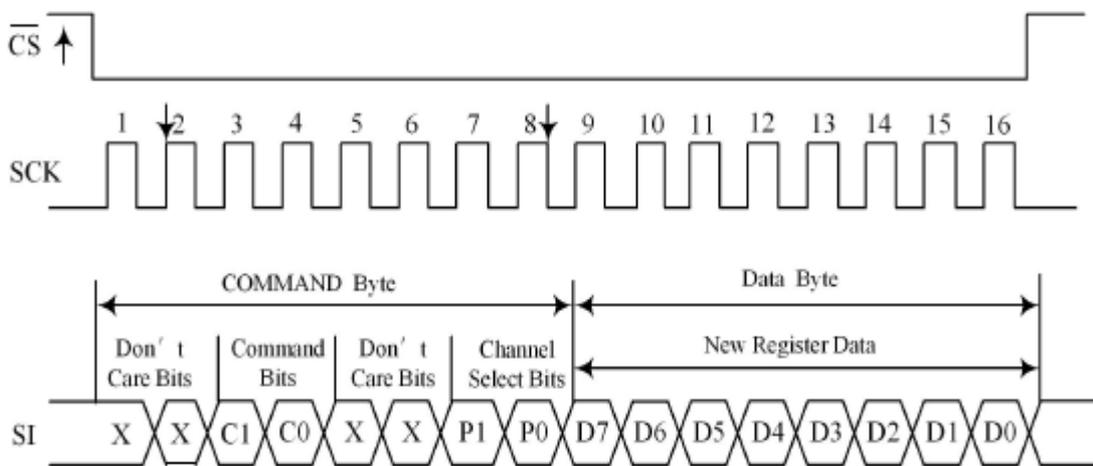


Figure 4. MCP41010 double byte instruction format

3.3 DDS module circuit design

3.3.1 Typical structure of DDS

The typical structure of DDS is shown in Figure 5. DDS technology is based on the sampling theorem, and its basic structure is composed of a phase accumulator, a waveform memory, a D/A converter and a low-pass filter [9]. Under the action of the clock, the phase accumulator starts to work regularly. PFSW (frequency control word) can control the number of relevant phases accumulated each time, and then feedback the phase information of the generated waveform to the referenced microprocessor. The waveform memory stores the phase and amplitude table of the waveform. The microprocessor

can query the amplitude information corresponding to the relevant phase by looking up the table and effectively output it to the D/A converter. The discrete amplitude information is sent to the D/A converter through the digital signal. The step wave is obtained after the conversion process of the analog signal, and then a certain signal waveform we need can be obtained under the action of the smoothing filter.

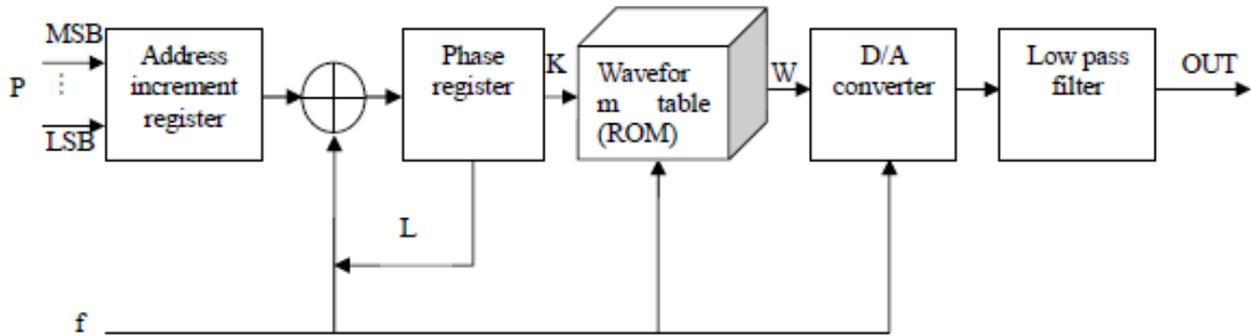


Figure 5. DDS typical structure diagram

3.3.2 The peripheral circuit design of the waveform generator

The internal circuits of AD9833 mainly include numerically controlled oscillator (NCO), frequency and phase regulator, SineROM, D/A converter, and voltage regulator. The core of AD9833 is a 28-bit phase accumulator, which is composed of an adder and a phase register, and the phase register increases the step size according to each clock, and the output of the phase register is added to the phase control word and then input into the sine look-up table address. The sine look-up table contains the digital amplitude information of a periodic sine wave, and each address corresponds to a phase point within 0-360° in the sine wave. The look-up table maps the input address phase information to a digital signal of sine wave amplitude, and drives the D/A converter to output analog. The main features of AD9833 are: frequency and phase can be digitally programmed; when the working voltage is 3V, the power consumption is only 20mW; the output frequency range is 0MHz-12.5MHz; the frequency register is 28 bits (under a 25MHz reference clock, the accuracy is 0.1 Hz); can choose sine wave, triangle wave, square wave output, without external components; 3-wire SPI interface; temperature range is -40°C~+105°C. The function of each pin is shown in Table 1.

Table 1. AD9833 each pin function table

Pin number	Pin symbol	Function Description
1	COMP	DAC offset pin, this pin is used to decouple the DAC offset voltage
2	VDD	Digital circuit power terminal
3	CAP/2.5	Digitally
4	DGND	Main frequency digital clock input
5	MCLK	Serial digital input
6	SDATA	Serial clock input
7	SCLK	Control input, active low
8	FSYNC	Simulation ground
9	AGND	Input frequency
10	VOUT	

The three waveforms, sine wave, triangle wave and rectangular wave, are output through the VOUT pin of the AD9833 waveform generator. The OPBITEN (D5) and mode (D1) bits of the control register are used to determine which output type the AD9833 waveform generator will provide. Its working mode is shown in Table 2.

Table 2. Internal working mode of AD9833

OPBITEN Bit	Mode Bit	DIV2 Bit	VOUT Pin
0	0	X1	Sine wave
0	1	X1	Triangle wave
1	0	0	DAC data MSB/2
1	0	1	DAC data MSB
1	1	X1	Keep

The interface design corresponding to the DDS module and the MCU main control module is shown in Figure 6.

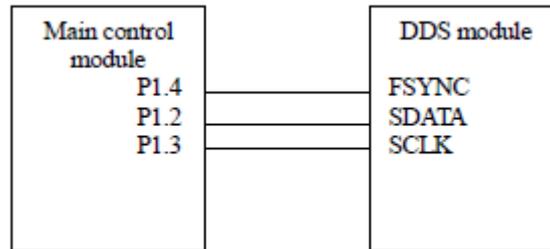


Figure 6. Module interface pin diagram

AD9833 waveform generator is a fully integrated direct digital frequency synthesis chip [10-13]. The chip requires a reference clock, a precision low resistance and multiple decoupling capacitors to digitally generate output waveforms up to 12.5MHZ. The typical value of the peak-to-peak value of the output signal of the AD9833 waveform generator is 0.6V, which cannot meet the design requirements. A waveform peripheral circuit needs to be added, and the module needs to have two functions: adjustable amplitude and amplification. Comprehensive considerations require the introduction of digital potentiometers and high-speed operational amplifiers. Therefore, on the basis of the waveform generator AD9833, the potentiometer MCP41010 is introduced to form a continuous and adjustable amplitude output circuit, and because the amplitude of the effective signal output by the digital potentiometer MCP41010 is small, the output amplitude needs to be continuously adjustable in the front On the basis of the signal, a high-speed operational amplifier AD8051 amplifying circuit is added. All three waveform signals output after adding peripheral circuits can achieve continuous adjustable amplitude. The peripheral circuit module design of AD9833 waveform is shown as in Fig. 7.

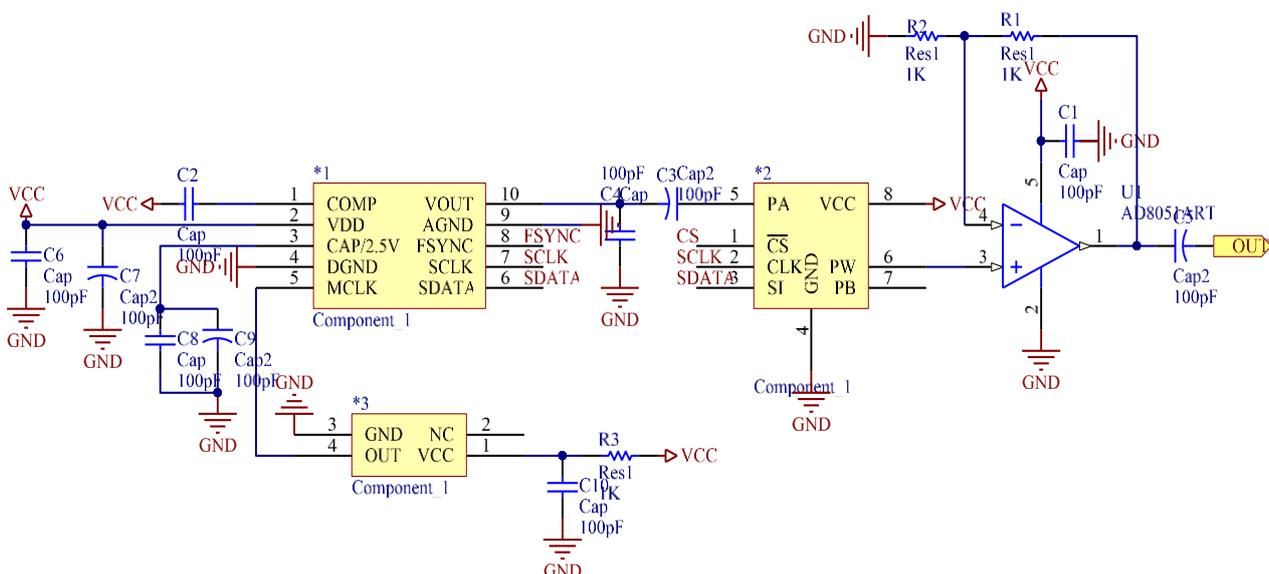


Figure 7. Waveform generator peripheral circuit design

4. Conclusion

The programmable signal generator system has the advantages of high integration, low loss, strong anti-interference ability and low delay. Its design is based on a DDS technology, plus a low-power single-chip AT89C52 main control module, through the digital potentiometer MCP41010 to adjust the potential, can achieve the adjustment of the output signal voltage peak value; the programmable signal generation The difficulty in the design of the signal generator system is that the signal frequency value generated by the signal generator needs to reach 12.5MHZ. The design found that the waveform signal generated by the AD9833 waveform generator has a voltage peak that is too low, and the output is only a peak voltage of 0.6~0.7V, which is far from reaching the 5V adjustable requirement of the output voltage peak. Because of this situation, this design introduces the high-speed operational amplifier AD8051 device, the purpose is to scale the output signal voltage peak, so that the output waveform signal can achieve 5V continuously adjustable.

The main problem faced by the software design part of the programmable signal generator system is how to realize the successful construction of the three-port connection between the microcontroller AT89C52 and the waveform generator AD9833, and to amplify the peak value of the waveform signal voltage output from the waveform generator AD9833 VOUT terminal. Finally, by consulting the relevant chip information, the problems existing in the design process are properly resolved. By adjusting the buttons, it is found that the three waveforms output by the system can be freely converted, and the amplitude and frequency of the output waveforms can be increased or decreased freely through the buttons. Within the frequency range of 10MHZ, the three waveforms are good and there is no obvious distortion; However, after the frequency range of 10MHZ is exceeded, after debugging, it is found that the output waveform sometimes has burrs, and the rectangular wave is especially protruding, indicating that the circuit software and hardware structure design is not perfect, and there are certain design defects, which leads to the final signal generator. There is a certain error in the output signal.

In short, the design of the programmable signal generator has been completed, and its main tasks and functions have been basically realized, but to make it reach the practical application level, more other factors need to be considered, such as temperature, dry humidity and signal electromagnetic field interference. Therefore, if you want to put it into actual production applications, you need to continue to study and improve on this basis.

References

- [1] Hu Xiaofeng, Wang Hongliang, Wang Chaojie, Chen Yibo, Design of a programmable multifunctional digital I/Q signal generator [J]. Science Technology and Engineering, 2016, 16 (29): 247-251.
- [2] Yu Dan. Design and implementation of signal generator system simulation [J]. Hubei Agricultural Mechanization. 2019(24):152.
- [3] Yang Yang. Design of Function Signal Generator[J]. Science and Technology Outlook, 2017.1.
- [4] Hu Huibin, Zheng Bin. Design of Programmable Multifunctional Signal Generator [J], Electronic World, 2016[14]:302-303.
- [5] Cui Jianpeng, Zhao Min, Jiang Fan. Virtual Arbitrary Waveform Generator Realized by DDS Technology [J]. Computer Measurement and Control, 20017, 11 (7): 553-555.
- [6] Chang Le. Design and research of low-frequency signal generator based on DDS[J]. Electronic Test, 2019(24): 10-11.
- [7] Ma Wenying. The design of triangle wave signal generator[J]. Science Technology and Innovation, 2019(20): 130-131.
- [8] Wang Menglong. Design of programmable signal generator based on MSP430 and AD9833[J]. Electronic Test Technology, 2018(23): 1-2.
- [9] Sun Yuxuan. Design of high-frequency signal generator based on DDS and single-chip technology[J]. Computer Products and Circulation, 2018(07): 112+117.

- [10] Li Yuqing, Tian Juan. Design and implementation of high-frequency sine wave signal generator based on DDS[J]. Journal of Tonghua Teachers College, 2020, 41(02): 5-8.
- [11] Zhang Qingbo, Pan Qingquan, Guo Liufei, Li Xiaoliang. Application design based on DDS multifunctional signal source[J]. China Equipment Engineering, 2019(24):167-168.
- [12] Ma Yakun, Li Guohua, Gu Xiaying, Gao Juchun. Continuously adjustable amplitude waveform generator based on AD9833 and AT89S52 [J]. Instrument Technology and Sensor, 2013(06): 32-34.
- [13] Mao Qun. Multifunctional signal source design based on DDS technology [J]. Journal of Xichang College (Natural Science Edition), 2018, 32(03): 88-90+115.