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Research on Vehicle Identification Technology Based on SOPC

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Abstract

In recent years, with the rapid increase of computing power and interpenetration and continuous development of many subjects, artificial intelligence has gradually entered the public's vision. Deep learning is an important means of artificial intelligence. This paper mainly studied and implemented how to apply the technology of deep learning on the System-on-a-Programmable-Chip platform to complete the function of recognizing and classifying the vehicle image data collected by the camera. The main content of the paper is as follows. Firstly, it introduced the knowledge related to deep learning and determined the CIFAR-10 data set. Based on this, the construction and training of Convolutional Neural Networks under the framework of caffe network and the way to use external data to test the reliability of the network were been realized. And the network reliability test and the extraction of important parameters of the convolutional neural network were performed. Next, a hardware platform based on SOPC-based camera data acquisition and display is designed. The platform provides hardware support for forward recognition algorithms for convolutional neural networks. At the same time, the forward recognition algorithm for convolutional neural networks was implemented by using C language on the operating system side. After this, by using the accelerator technology of the SDSOC development platform, the C language functions that affect the speed of the system was converted into the hardware circuit of the FPGA, and the entire forward identification algorithm was accelerated. Finally, the entire system was tested and the experimental and the results were analyzed to confirm that the system can achieve the desired function.

Keywords

SOPC; Vehicle Identification; Deep Learning; Convolutional Neural Network; Accelerator.

1. Introduction

In recent years, with the rise of GPU and the improvement of computer computing power, the technology of computer vision and image processing has been developed rapidly. At the same time, with the continuous development of society, a variety of vehicles begin to popularize in our life. The identification of vehicles in the natural environment is an important part of intelligent transportation system. At the same time, the cameras on each traffic road can collect the real-time transmission image data. By using various algorithms to process these image data, we can extract the image feature information, help solve the traffic problems, and store the processed data for big data analysis.

Image classification and recognition inevitably involves deep learning. In recent years, as learning problems become more abstract and complex, the network scale of deep learning is also increasing, and the complexity of computing and data is also increasing. Mishkin and Matas (2015) pointed out in the paper that GPU has the problem of high power consumption, and it is unable to apply deep learning on miniaturized devices. How to implement high-performance and low-power related deep learning algorithm has become a research hotspot.

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FPGA is also called field programmable gate array, which has the characteristics of high performance, low power consumption and programmable, which makes it one of the commonly used acceleration means. The experimental results of Wang Jia (2014) also show that compared with GPU, the performance of FPGA based neural network accelerator has an average improvement of 0.22 times, while the area of gpuc 2070 is only 0.56% of the on-chip area of gpuc 2070. FPGA is more convenient for miniaturization of design. This paper uses the zynq chip produced by Xilinx company. This is a FPGA with embedded ARM hard core. This architecture enables programmable hardware and software systems to work together. This programmable system on chip is also known as SOPC (system-on-a-programmable-chip). With this SOPC, the most powerful forward recognition algorithm can be realized in arm. At the same time, sdsoc development tools are used to implement the functions that affect the system running speed, so as to complete the targeted acceleration of the algorithm.

It can be seen that deep learning is very mature in terms of algorithm and network structure, so when applying deep learning, more efforts should be put into hardware acceleration technology (Yang Xuyu et al., 2016). The accelerator designed by Yu Qi implements both the forward recognition algorithm and the reverse training algorithm of deep learning in hardware, but the pure hardware implementation idea does not achieve good performance. Then we can change the way of thinking, use mature computer training technology to train enough reliable deep learning network, and extract the important parameters that determine the performance. SOPC, which works together with software and hardware, uses these parameters to realize the forward recognition algorithm of deep learning network, and only accelerates the algorithm with high resource occupation by hardware. This design idea can be used as far as possible Under the premise of ensuring network performance, it uses less hardware logic resources and realizes deep learning application with low power consumption.

2. Overall framework

According to the design requirements of the system, the overall design scheme of the system can be obtained. First of all, it is necessary to determine the network framework and data set needed for deep learning, and then use computers to complete the training of deep learning network model (Xu Guangqiang, 2017). After using the test network to determine the reliability of the model, the important parameters of the network model are extracted for standby.Secondly, we need to use hardware development tools to complete the hardware network platform supporting camera data acquisition, transmission and display in the programmable logic end of SOPC development board, and realize the data interaction between the programmable logic end and the operating system side.

Finally, we need to use sdsoc to complete the deep learning forward recognition network in the SOPC operating system by using the important network parameters extracted before and the image data provided by the hardware platform, and accelerate the high occupancy function, so as to realize the application and acceleration of deep learning on SOPC.

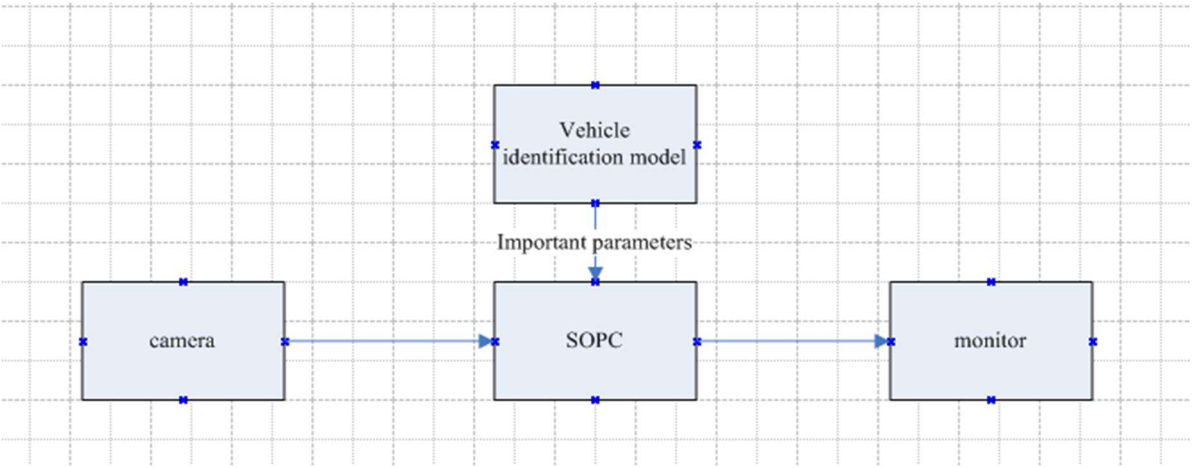

Figure 1. Overall framework (System)

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The main process of the hardware platform is: firstly, the Bayer image collected and input by CMOS camera is converted into RGB image, and then the RBG image is input into m together with the synchronization signal and the image starting signal_ AXI_ Full bus control IP core, in M_ AXI_ In the full control IP core, the input RBG image data is processed across clock domain through asynchronous FIFO through custom programming, and then, according to Axi bus transmission protocol, through Axi_ Full bus is transferred to the memory of zynq by DMA, and then the data is written to DDR3 by arm DDR3 driver.

HDMI via Axi_ The full bus sends a request to PS (processing system operating system) to read DDR3 data. After receiving the request, the PS side takes out the image data of the specified address and passes through Axi_ After receiving the data from Axi bus, HDMI first uses FIFO to process the received data across clock domain, and then splits RGB data into 8 bit data of RGB three channels. After 8b to 10B, 10b to 1b, serial to differential processing, and finally output to the display.

After the image data is compressed in PS terminal, a series of convolution operations and recognition are completed by algorithm accelerator. The recognition results will cover the specified position of the image and will be sent out to the display along with the image for display.

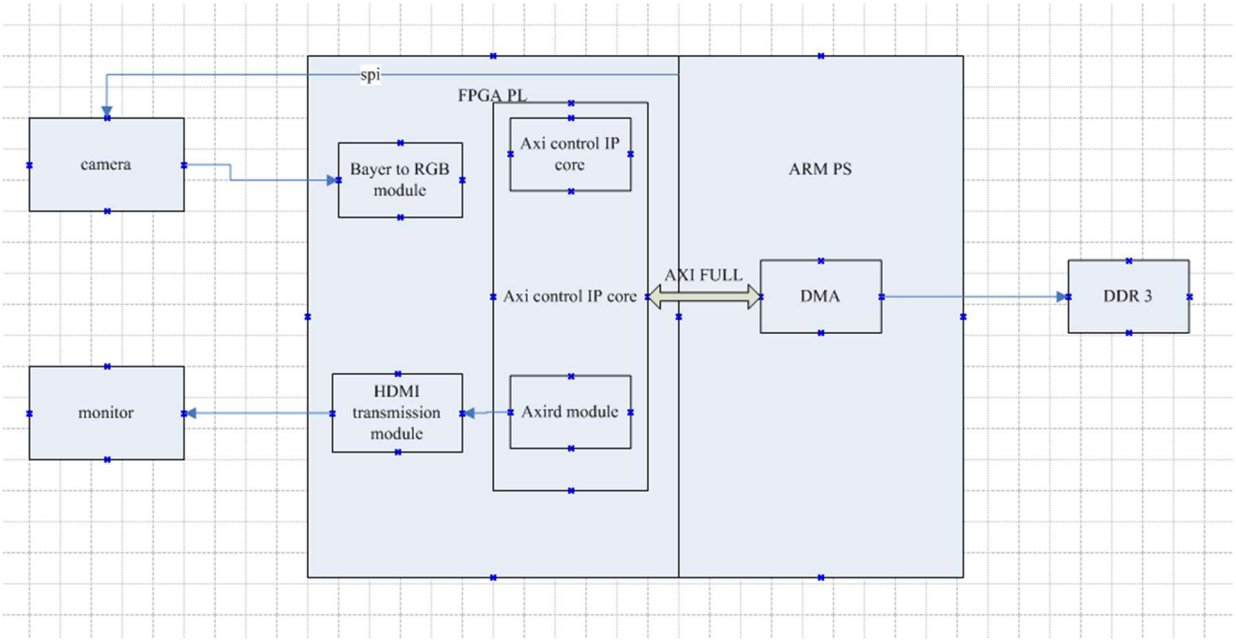

Figure 2. Overall framework (Hardware)

2.1 Model parameter extraction

After testing the network, the reliability of the network model is determined. Next, we need to extract the weight and bias value of the model to save the acquired knowledge for the hardware platform algorithm.

Here we can use the python interface provided by Caffe framework for network parameter extraction, and use Python script to extract the parameters such as bias value and weight in reliable model for C convolution code of ARM core. In order to meet the requirement that the extracted array can be used by C language, it is necessary to change the extracted array into the array in C language form. This paper deals with the conversion between Python array and C language array, as long as the symbol representing Python array is replaced by {} symbol representing C language array.

The layer of parameters to be extracted includes the weight and bias parameters of convolution layer 1, convolution layer 2 and full connection layer.

Specific Python code can refer to the directory: 6. Convolution layer 1 parameter extraction Python script; 7. Convolution layer 2 parameter extraction Python script; 8. Full connection layer parameter extraction Python script.

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2.2 Model training

After the design of user-defined network structure and parameter initialization file, the whole network needs to operate. The whole neural network needs to run the training script for network training to start. The training script is mainly used to call the network training tool provided by Caffe and to specify the initialization parameter file for activating training. In essence, it serves as a connection channel between training tools and initialization files. When the training is interrupted, the system will store the training model. When you want to continue training from the break, the script also needs to specify the model the system saves at the break. Specific code please refer to appendix: 3. Training script.

From the learning report of the network, we can see that the recognition accuracy is only 0.0936 at the beginning of training, and it has reached 0.4699 after 400 training times. The loss of the function converges from 2.30321 to 1.37775. This shows that the network began to carry out correct training, the system to gradually reliable direction transformation. The training network report is shown in Figure 3.

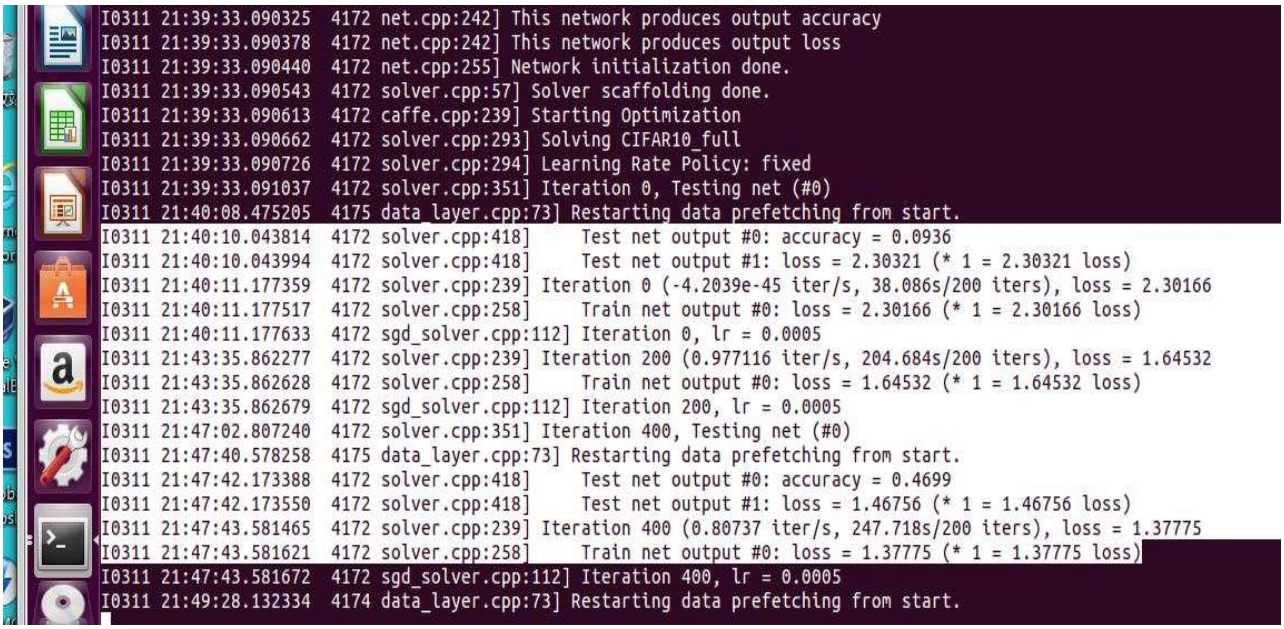

Figure 3. E-learning report at the beginning of training

Figure 4. E-learning report when training 16000 times

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When the network is continuously trained to 16000 times, it can be seen from the training report shown in Figure 4 that the recognition accuracy has reached 0.7281, and the loss of the function converges to 0.836234. At this time, the convolutional neural network trained based on cifar-10 data set has high reliability.

Through the above experimental phenomena, we can see that the convolutional neural network based on cifar-10 under the Caffe network framework can realize the recognition and classification function of images in the dataset through continuous training.

From the reliability test results, it can be seen that although there are still wrong identification results, the system has been able to concentrate the identification results on a single tag without the problem of multiple controversial tags.

2.3 Implementation of volume calculation method

HDMI module is mainly used for high-speed image transmission. The workflow is to convert 24 bit RGB image data into differential signal of corresponding channel according to the transmission protocol, and then transmit the image data to the display through HDMI connection line for display. The architecture of HDMI module is shown in Figure 5.

The data of HDMI module is requested to the corresponding position according to the line counter, field counter and line field synchronization signal

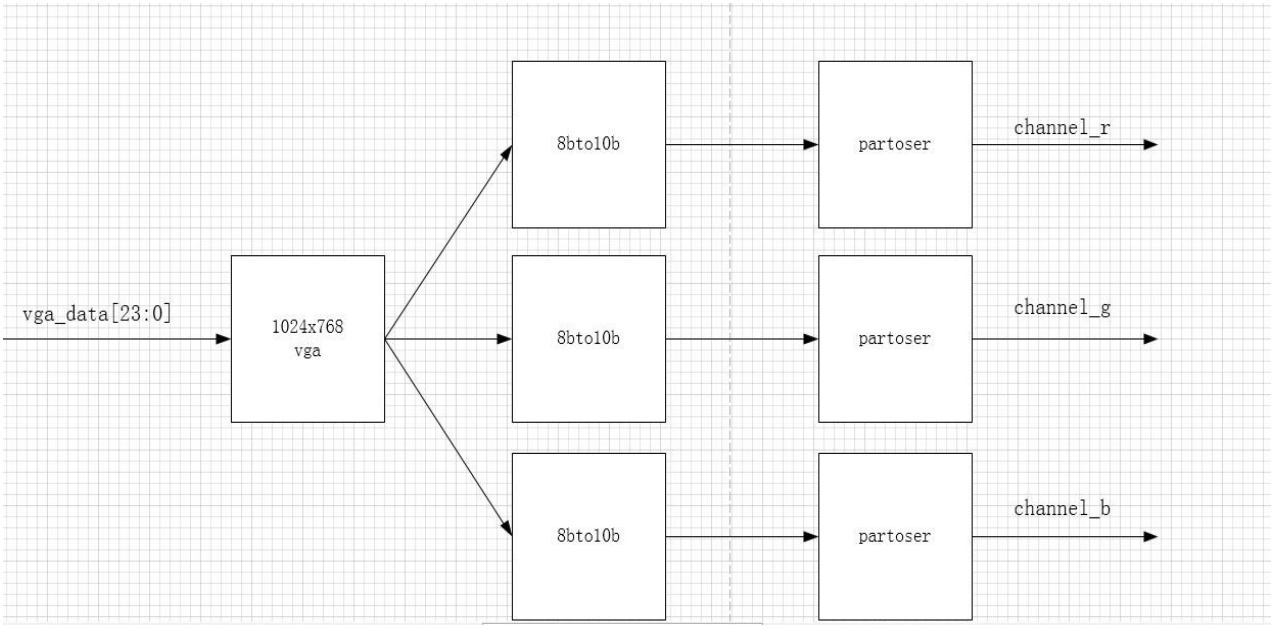

Figure 5. HDMI

What should be noted here is: since HDMI transmits image data quickly and the module works in high frequency environment, the output signal needs to be converted into differential signal to maintain the reliability of data. Therefore, in a clock cycle, each channel needs to convert the received 10bit data into 10 1bit differential signals, so the working clock frequency of our conversion operation needs to be 10 times For the clock frequency of receiving 10bit data, we can use double edge sampling method, and use the rising edge and falling edge of the clock to send data at the same time. Therefore, in fact, the clock frequency of 10B to 1b is only 5 times of the previous system working clock.

3. System testing

In order to complete the test of the whole vehicle identification system, it is necessary to provide the data source of the vehicle image, the camera data acquisition module, the SOPC hardware development board for realizing the recognition function and the display for displaying the recognition results. The specific test environment is shown in Figure 6.

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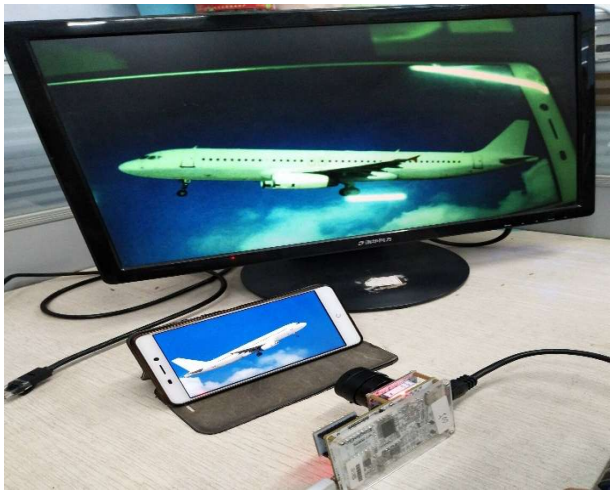

Figure 6. Testing environment

3.1 Test result

Four correct recognition results are shown in Figure 7(a) and Figure 7(b).

(a) (b)

Figure 7. Four correct recognition results

Observe and count the recognition results of different types of vehicles on the display screen. Although there are still wrong identification results, the system can basically complete the classification and recognition of vehicles. It can be considered that the whole design system has basically completed the intended goal.

4. Conclusion

With the continuous development of artificial intelligence theory and computer hardware, deep learning application is gradually familiar with and accepted by the public, but also gradually changes people's daily life. Vehicle recognition technology applied to deep learning can provide support for its and big data analysis.

Then, this paper uses vivado development tool to build a hardware platform supporting camera data acquisition, transmission and display in FPGA side of zynq. Combined with sdsoc development tool, the convolutional neural network forward recognition algorithm is designed in arm side of zynq, and the core algorithm is accelerated to realize the deep learning application of vehicle recognition based on SOPC. Finally, the design is tested and the experimental results are analyzed. It is confirmed that the system can basically complete the recognition and classification of vehicle images collected by the camera.

This paper mainly uses the characteristics of software and hardware cooperation of zynq SOPC chip, realizes the forward recognition algorithm of convolutional neural network in arm, and accelerates the core algorithm in FPGA. This design is different from using FPGA to implement all the forward

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and backward algorithms of convolutional neural network, but it uses computer to share the task of training convolutional neural network, and uses hardware to complete the most important recognition function of deep learning. This kind of deep learning application scheme, which combines the powerful computing power of computer and the advantages of SOPC miniaturization and low power consumption, can provide good support for the hardware scheme which only needs to realize the recognition function.

However, there are still some aspects to be improved in this design

We can reduce the consumption of FPGA hardware resources by changing floating point number to fixed number. The extra hardware resources can be used to improve the parallelism of the acceleration algorithm and reduce the identification system delay. In addition, vector filter or quantization coding can be added to reduce the loss of image features and increase the success rate of recognition.

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