Design of Multi-channel Signal Acquisition System Based on FPGA

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Abstract

This paper mainly introduces the design of a multi-channel sampling controller with FPGA, and uses VHDL language to design a finite state machine to realize the control of AD7892. Since the characteristics of the FPGA device are high-speed operation, an audio signal is selected for the analog signal. The function of the FPGA is very powerful. In this system, the functions of the AD channel selection part and the serial output control module are integrated into the FPGA device, so that the peripheral circuit of the whole system is simple and the system stability is strong. The configuration mode of the FPGA adopts the passive serial mode, which enhances the scalability of the system. The output mode is optional and can be adjusted according to specific needs. This paper mainly introduces the overall structure of multi-channel system, the principle and design method of each component, the FPGA software design part, the debugging and application of the system.

Keywords

Audio amplification,FPGA,VHDL, AD7892,finite state machine,multi-channel control.

1. Introduction

The importance of data acquisition in modern industrial production and scientific research is increasingly prominent, and the requirements for real-time high-speed data acquisition are also constantly increasing. In high-speed, high-precision measurement such as signal measurement, image processing, and audio signal processing, it is necessary to carry out High speed data acquisition.

FPGA (Field Programmable Gate Array) is a very large-scale, ultra-high-speed programmable logic device widely used in recent years. It has a breakthrough in the design of digital systems due to its high integration, high speed, and programmable online system. Sexual change has greatly promoted the singulation and automation of digital system design, and improved the design cycle, design flexibility and reliability of single-chip digital systems. It has a wide range of applications in ultra-high-speed signal processing and real-time measurement and control. The Hardware Description Language HDL is a language that uses formal methods to describe digital circuits and systems. VHDL is one of several representative languages of the hardware description language. VHDL is mainly used to describe the structure, behavior, function and interface of digital systems. Compared with other hardware description languages, VHDL has stronger behavior description ability, which determines it becomes the best hardware description language in system design field.

This design uses FPGA and other auxiliary circuits as the basis of the hardware circuit, and implements the sampling system by software programming in VHDL language to realize the data acquisition of audio signals.

2. Overall system design

The hardware circuit of the system includes a multi-channel sampling controller designed by the FPGA and a corresponding channel selection circuit and an A/D conversion circuit. Since the audio signal is sampled, it is necessary to design an audio amplification and filtering circuit. The system components are shown in Figure 1.1:

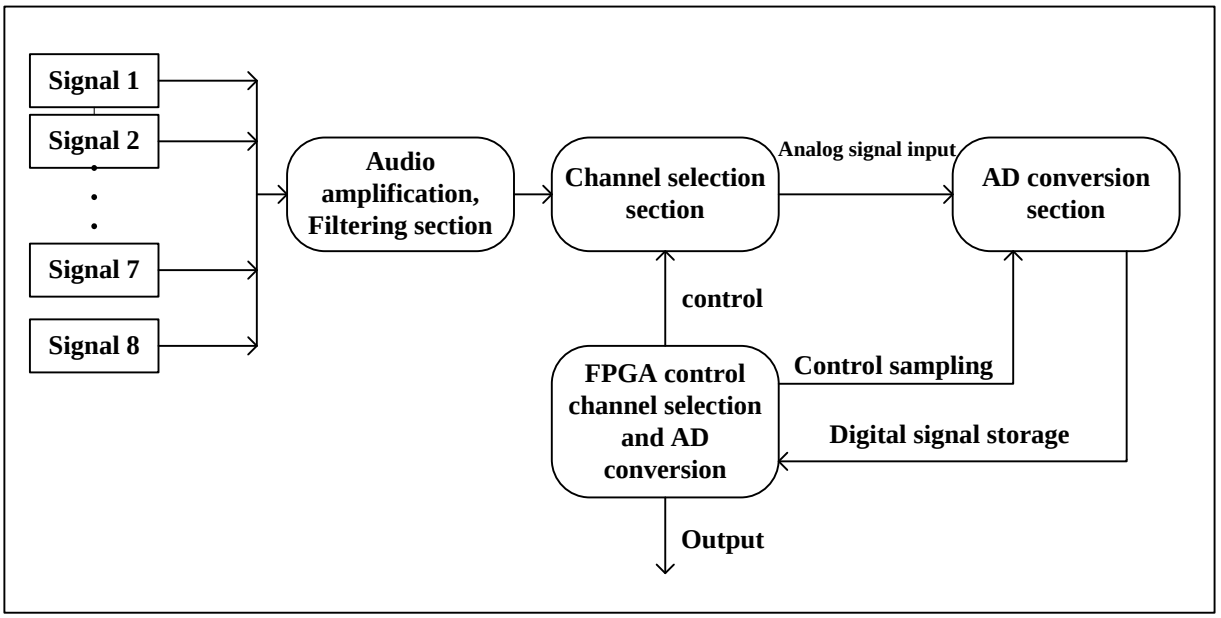

Fig. 1 System overall design

2.1 Design Scheme Argument

A 3-bit octal counter is implemented by FPGA. The counting pulse is the latch signal of the FPGA latching AD conversion data, and the output of the counter is used as the address of the data switch CD4051. The finite state machine is used to control the AD7892, so the circuit implementation is relatively simple, and the sampling rate of the AD7892 can reach 500KHz, and 8 channels of simultaneous 8-channel audio signal acquisition can be realized. At the same time, the FIFO module is used to store the digital data in the queue first, while writing data to the queue and reading the data from the queue, thus playing a role of caching the digital data, and speeding up the operation of the entire system.

At the same time, the state machine is easy to form a synchronous timing logic module with good performance. In order to eliminate the glitch in the circuit, there are many design options available in the state machine design. The read and write operations of the FIFO queue can be completed in one cycle, which acts as a cache. This speeds up the operation of the entire system, solves the "bottleneck problem" of sampling and storage, and makes more efficient use of the resources of the FPGA chip.

3. Hardware system

It can be concluded from the overall design of the above system that the system can be divided into four parts, namely audio amplification, filtering part, FPGA control part, AD sampling circuit, and FPGA hardware circuit design. The FPGA control part is the main part, which involves AD sampling control, channel selection control, serial output mode selection module and FIFO module introduction.

3.1 Audio amplification, filtering part

The frequency range of the sound that can be discerned by the human ear is: 20Hz-20KHz, so there is a bandwidth requirement for the amplifier of the audio amplifying part, and the amplifier is required to be broadband. Therefore, this design uses a high-speed low-noise op amp NE5532 dedicated to audio amplification as an amplifier for the amplification part. The filtering section is an active

bandpass filter that filters out low frequencies below 20 Hz and high frequency interference above 20 kHz.

In practical circuits, the input signal often contains some unnecessary components due to interference and other reasons, and should try to attenuate the interference to a sufficiently small extent. In order to separate the signals we need from the aliasing signal, a filtering circuit is specially designed. The filter includes a passive filter composed of reactive elements L and C, an active filter composed of an integrated operational amplifier, and a crystal filter. Because the passband frequency range of this acquisition signal is 20Hz-20KHz, it is a wideband filter, so a low-pass filter and a high-pass filter cascade are used to realize band-pass filtering. Its circuit structure is shown below:

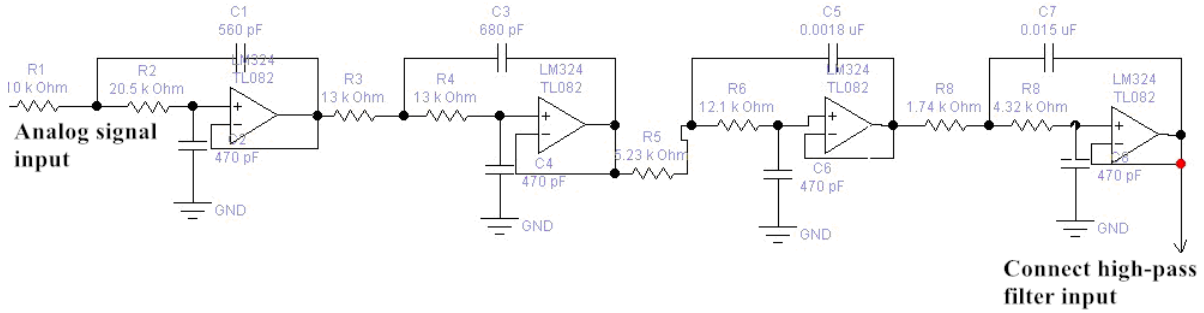

Fig.2 Low pass filter circuit diagram

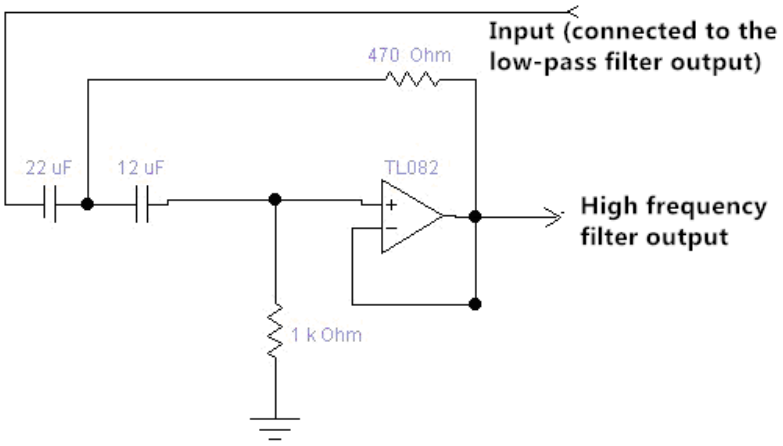

Fig.3 High-pass filter circuit diagram

3.2 AD sampling

Since the frequency range of the audio that can be recognized by the human ear is 20 Hz-20 KHz, according to the Shannon sampling theorem, the digital signal after sampling can be restored to an analog signal, and the sampling frequency must be twice the frequency of the analog signal, that is, this time The sampling frequency of the sampling system should be designed at 40KHz, and the sampling frequency of the audio signal of the general CD format is 44.1KHz. Since it is the sampling of 8 channels, the lowest sampling frequency of the AD chip should be 44.1KHz8=352.8KHz, so choose The AD7892 has a sampling frequency of 500KHz.

The AD7892 is a successive approximation 12-bit high-speed ADC with sampling protection function produced by ANALOG DEVICE of the United States. The AD7892 analog-to-digital converter has the following features:

(1) Single power supply operation (+5V);

(2) incorporating a sample-and-hold amplifier;

(3) It has a high-speed string and parallel interface.

The circuit connection of the AD7892 to the sampling system is shown below. The purpose is to convert the audio input analog signal into a 12-bit digital signal. The circuit uses the parallel output mode of the AD7892AN-1, and its acquisition speed is designed to be 500kSPS.

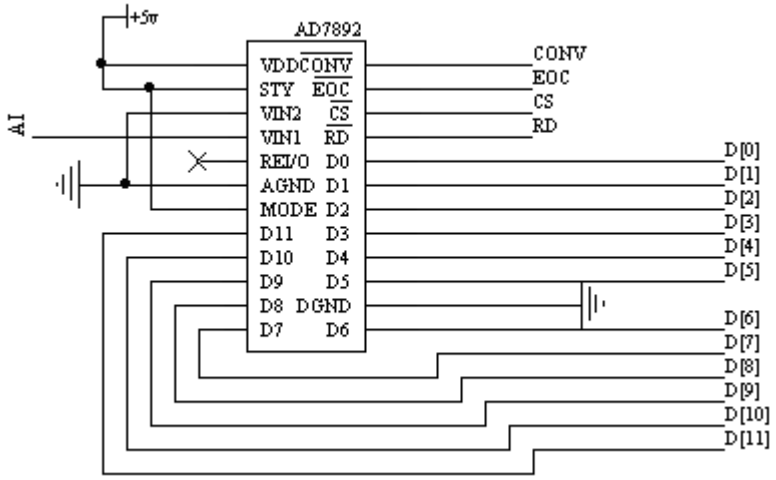

Fig.4 AD7892 sampling system connection circuit diagram

4. FPGA Control Section

4.1 Channel Selection Module

The channel selection part is a binary modulo 8 counter. The counter clock is the latch signal of the AD digital signal. Each time the data is latched, the counter will be incremented once. The CD4051 selects the audio signal of the next channel for acquisition. The design of the graphic in VHDL language in Quartus II is shown below:

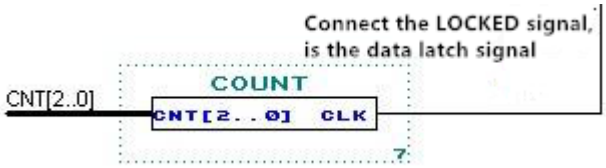

Fig.5 Channel selection section

The corresponding channel is selected by CNT[0] to CNT[2], and the output of CD4051 is the last audio signal to be sampled by AD. For example, if CNT[0]CNT[1]CNT[2]=“000”, the first channel audio signal is selected for AD sampling. The focus of this part of the implementation is to count the digital latch signal, the output of the counter as the channel selection address of the CD4051.

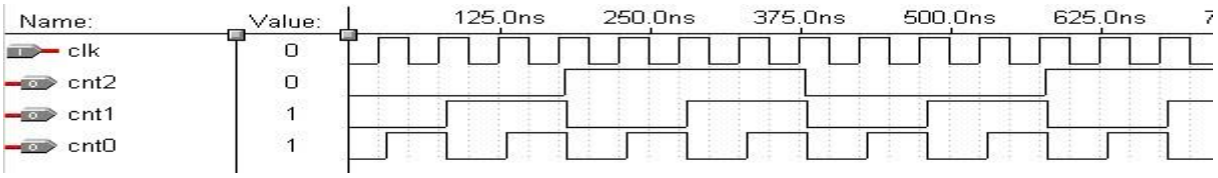

Fig.6 Channel module simulation

4.2 AD7892 Control Section

The control part of the AD7892 is mainly realized by a finite state machine. By observing the working sequence of the AD7892, the control signal of the AD is described by the finite state machine, so that

the AD chip can work. The state transition diagram based on the timing diagram of the AD7892 is shown in the figure:

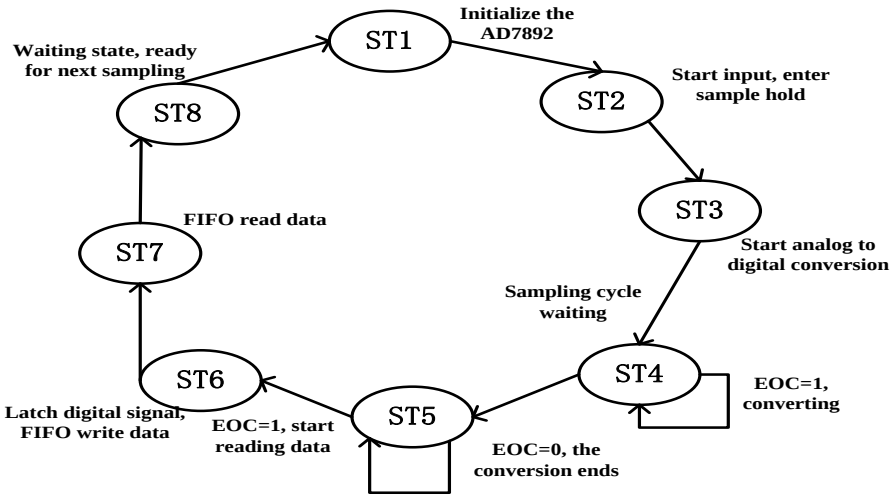

Fig.7 AD sampling state transition diagram

In a complete sampling period, the first time the state machine is started is the timing process with CLK as the sensitive signal. Then the two combined processes COM1 and COM2 are simultaneously started because they use the same signal current_state as the sensitive signal. The last time it is started is the latching process, which is started after the state machine enters ST6. That is, LOCK generates a rising edge signal, which starts the process LATCH1 and puts the AD7892 in the 12-bit data and channel of this sampling period. The selected 3-bit data is latched into the register, and the FIFO memory reads stable and correct data from the Q terminal. After entering the next state, the FIFO reads the data to the q-end again, so that one sampling period is completed. The waveforms simulated in the Quartus II are shown below:

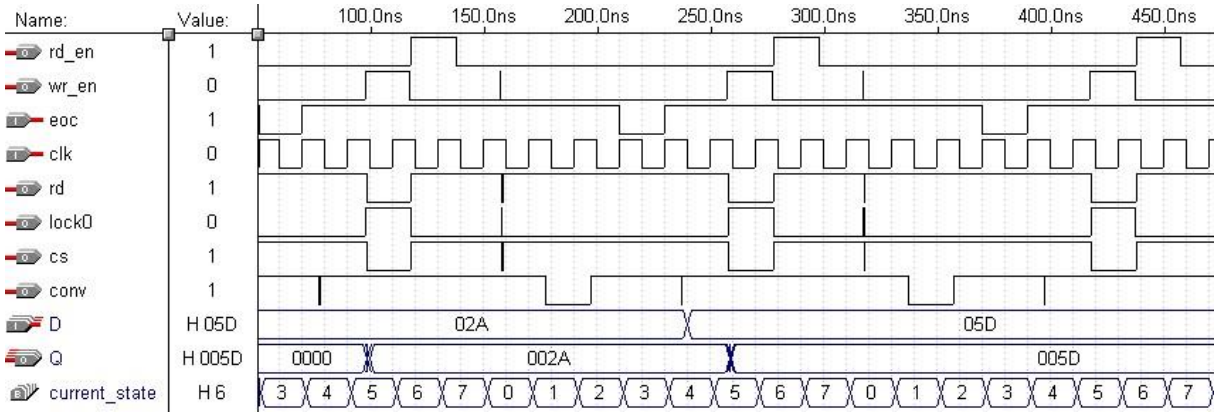

Fig.8 AD sampling control simulation waveform

It can be seen from the simulation waveform that the control signal conforms to the timing of the AD7892, and the AD can be sampled and controlled, and the latched signal of the data also meets the design requirements of the topic. But as you can see from the simulation diagram, these signals are a lot of burrs. Because the glitch is very short, it is usually a few nanoseconds. It is basically impossible to meet the data establishment and holding time, which will not affect the whole system. So we choose to ignore.

4.3 Output Control

The data output from the AD control module is parallel 16-bit data. The principle of serial output is: continuously select the output parallel 16-bit data through a 16-select 1 data selector. The data selector's selection signal is a counter output of the binary modulo 16 of the system clock count. Convert parallel 16-bit data to serial data. Whether the serial output or the parallel output can be

realized by the external input signal P/S. If P/S is low level, the selector of 16 select 1 is strobed, and the output of 16 AND gates is disabled. At this time, the serial output is If P/S is high, the 16-selector selector is disabled, and 16 AND gates are turned on at the same time. This is a parallel 16-bit output. The output mode can be selected to make the system widely used. The serial output can be used for the acquisition of communication signals, which is convenient for modulation and transmitted to the remote receiver. The remote receiver demodulates the collected data. The parallel output mode can pass. The high-speed memory puts the collected signals on a microcomputer or other processor, and performs corresponding control according to the collected data.

4.4 FIFO module

This design project uses the FPGA to directly control the AD7892 to achieve high-speed signal acquisition of the audio signal. After sampling one cycle, the data is stored in the memory, and then the data is read out from the memory and displayed. The sampling memory is internally used. The FIFO stores data because the high-speed AD sampled data memory requires a short storage time, while the FIFO write time is only one clock cycle, which meets the design requirements.

4.5 Power Module

Due to the high operating voltage requirements of the chip, the three-terminal regulator LM317 is selected. The LM317 is a three-terminal adjustable regulator IC from National Semiconductor. It is very simple to use and requires only two external resistors. Set the output voltage. In addition, its linear regulation and load regulation are better than standard fixed voltage regulators. It also has built-in overload protection, safety zone protection and a variety of protection circuits. Since the pin voltage of the I/O port of the design FPGA chip is set to 2.5V, the voltage of the LM317 is designed to be 2.5V to provide the working voltage for the entire FPGA chip.

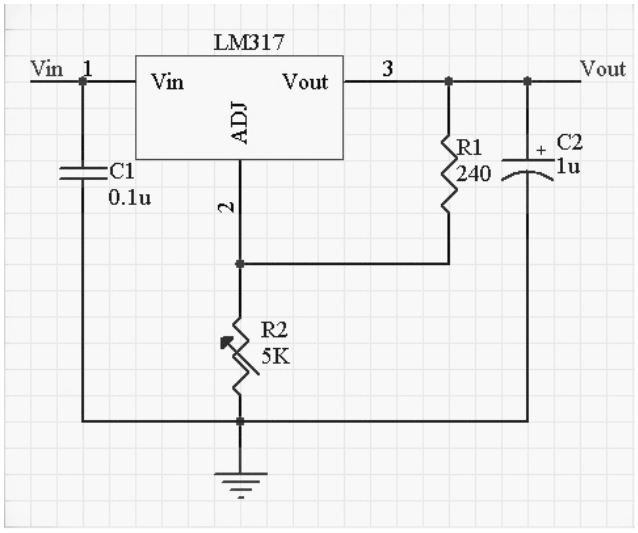

Fig.9 Typical Application of Three-Ended Regulator LM317

5. System debugging

System debugging requires experimental tools: oscilloscope, regulated power supply, EDA test bench, PC, ByteBlaster (MV) download cable. Connect the whole sampling system according to the connection order of each module in Fig.1, respectively connect the ±12V amplifier working voltage, +5V AD sampling voltage and +2.5V FPGA chip working voltage, and select serial port to select serial output. The shorting cap is shorted so that the input to the device is low. Connect the oscilloscope to the serial output port, connect the print parallel port on the PC and the download port on the hardware circuit board with the download circuit on the EDA test bench. You can see that the oscilloscope has high level output. The serial port selection port is selected as the parallel output, that is, the shorting cap is disconnected, so that the input to the device is high level, and any one of the

selected ones is connected to the oscilloscope, and the high and low level outputs can also be seen. The basic realization of the entire high-speed multi-channel sampling system can be confirmed by debugging, and the online debugging is completed.

6. Conclusion

This design uses FPGA to realize the sampling system, so the system has the characteristics of high speed, stability, low power consumption, etc. The audio analog signal is amplified by the amplifier NE5532, after 8 channels are selected, the filter is filtered, and the high frequency interference signal is filtered out. The interference of the low-frequency interference signal, then enter the AD7892 for AD sampling, the sampled 12-bit data is stored through a FIFO queue, and finally the digital signal is read out from the FIFO, and displayed on the oscilloscope under the selection of the serial-output mode. The experiment proves that the FPGA-based multi-channel signal acquisition system designed in this paper has strong feasibility.

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