Video transmission based on FPGA

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Abstract

This article chose the video standard DisplayPort 1.2, which can reach 21.6Gbps in four channels, meeting high resolution and high performance video requirements. Supporting DisplayPort means higher system bandwidth requirements, and the problem brought by the increase in resolution is that the bandwidth of the required memory is geometrically increased, and the FPGA chip becomes the transmission DP1 due to its own editability characteristics and rich logic resources. 2 video carrier. However, high-performance high-resolution video transmission based on FPGA still needs to solve the problem of increased logic in FPGA and increased power consumption of platform, high-speed signal transmission, decoding, and signal integrity of high-speed signals.

Keywords

FPGA, verilog, DisplayPort1.2,

1. Introduction

Originally the VGA interface, because CRT occupied the entire market at that time, the transmitted signal was only the horizontal scanning line, which is an analog signal, not the digital signal on the LCD today. Therefore, although the VGA is very outdated, it is still a lot of manufacturing. The minimum standards supported by the factory,

Since then, with the large-scale popularization of LCDs, DVI interfaces have also appeared. Since the LCD is completely different from the previous CRT, the CRT receives the analog signal, and the LCD accepts the digital signal. If the VGA is transmitted to the LCD as an analog signal, it needs to be converted into a digital signal in the LCD. The conversion caused a loss of detail in the video transmission, so the DVI interface appeared.

DVI English is called Digital Visual Interface and is based on the PanalLink interface technology, which allows uncompressed digital video to be transmitted to the display device.

Following the release of the next-generation HDMI (High Definition Multimedia Interface) digital interface, as a full digital impact/sound transmission interface, it can transmit high quality uncompressed audio and video signals, since the same cable can be used for audio and video signals. Transmission, which greatly simplifies the installation of the system, however, HDMI is not without its shortcomings. Because it is a product of the joint organization of commercial companies, it has to pay the license fee, which is not conducive to the later development of HDMI.

In this case, the DisplayPort digital interface is available. DisplayPort draws on the advantages of HDMI. It fully realizes the audio and video line, and the transmission bandwidth that can be supported is no less inferior to HDMI, and no license fee is required. It has gained wide support from the industry.

2. Organization of the Text

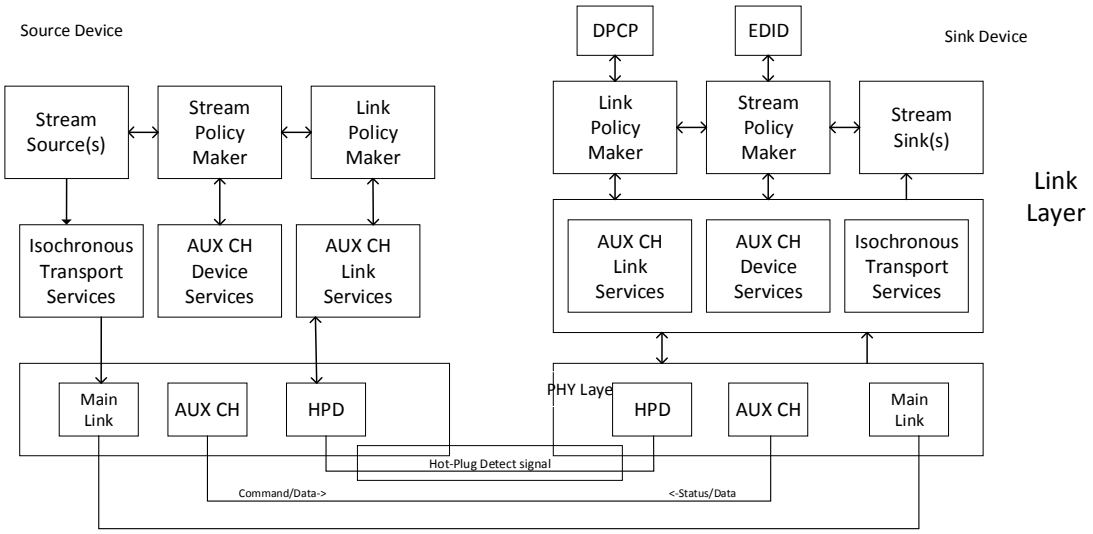
2.1 Basic introduction of the displayport1.2

The DisplayPortTM standard specifies an open digital communication interface that can be used internally, such as an interface within a PC or monitor, and an external display connection. Suitable external display connections include the interface between the PC and the display or projector, between the PC and the television, or between a device such as a DVD player and a television display.

2.2 Principle of displayport1.2

The DeplayPort 1.2 protocol can be divided into the receiving end (RX) physical layer, the receiving end (RX) link layer, the transmitting end (TX) link layer, and the transmitting end (TX) physical layer. As shown below

Figure 1-2: shows the layered architecture of DisplayPort.



Layered Architecture

The physical layer functions to receive parallel data from the link layer, convert the parallel data conversion to a serial data stream, and serially send it to the device or host. Control video and audio stream speed through data and control. Since the video and audio streams are mapped to the DP1.2 interface, the clocks are not synchronized, so time base conversion is required.

The main function of the link layer is to transmit and receive data packets. The data signal and the control signal sent by the TX physical layer are transmitted to the RX physical layer, and the link layer only needs to send and receive data, and does not know the contents of the data packet. Therefore, its function is to encode, verify, and verify and decode the lower layer data.

Upstream to downstream virtual channel mapping (also known as "DP router": around this central module is the DP receiving module and DP transmitting module, and each DP module is divided into "data plane" and "control plane"

2.3 Main link

One, two or four AC-coupled pairs of differential pairs form the primary link. The primary link supports three different rates, a standard rate of 5.4 Gbps, a one-half standard rate of 2.7 Gbps, and a quarter standard rate of 1.62 Gbps, while specifying that each operating channel must maintain the same rate. Although the speed of the link is separate from the pixels, it also has a certain relationship. The key to determining the rate is the ability of the sender and receiver as well as the quality of each channel. As shown in the figure below, the four channels on the transmitter are independent of each other and will be processed in the link layer due to the clock difference caused by the transmission.

2.4 AUX Channel

Each DP has a proprietary bus, the AUX Channel, for the handshake between the source and the sink, since source is the control device of the process, which makes a request for the sink. The only way for the receiving end to communicate with the transmitting end is to transmit a pulse in the Hot Plug (HPD) signal.

The auxiliary channel consists of an AC-coupled double-ended differential pair. Manchester coding is used as the channel coding for the auxiliary channel. The clock is also extracted from the data stream and is also consistent with the primary link. At the same time, the auxiliary channel is duplex and bidirectional. The receiving end is the main and the transmitting end is the auxiliary. The receiving end can switch the signal to the HPD to interrupt the signal of the transmitting end. Not only that, the auxiliary channel is capable of guaranteeing a rate of 1 Mbps on a data line of 15 meters or more with a delay of no more than 500 us.

The auxiliary channel is a key part of the communication. The key to understanding the handshake process is also to record the auxiliary channel communication.

2.5 Hot plug detection

Hot plug detection is used to implement link configuration and management functions.

When hot plugging is detected, the transmitting device configures the connection state through the connection alignment, and the DisplayPort transmitter and receiver determine the accurate drive current and equalizer level through the handshake protocol of the auxiliary channel, according to the detected accurate channel connection rate. Start the correct number of channels

After the link is aligned, during normal operation, the receiving device notifies the link state of the change, for example, the hot plug signal is initiated, resulting in loss of synchronization, which will result in an interrupt request, and then the transmitting device checks the connection status through the auxiliary channel, taking Corrective action, this closed-loop connection operation, improves the robustness and interoperability of the transmitting and receiving devices.

3. Key technologies and implementation approaches

3.1 Key Technologies

a) 2560X1440@60Hz video (true color 32bit) stream has about 7Gbps data traffic. In order to handle such high-speed data traffic, it must require extremely high-speed data interface and strong line-rate real-time processing capability;

b) for two 2560X1440@60Hz video (true color 32bit) streams with around 14Gbps of data traffic (plus additional control overhead, such as MST headers, and asynchronous clock offsets, which actually require more data traffic), Must require a higher speed data interface and greater processing power;

c) For the entire data transmission channel, there is processing of the asynchronous clock and transmission of the video stream between the asynchronous clock sources. The clock ls_clk of the interface needs to be larger than the stream clock strm_clk, and the TX and RX clocks of the platform are also asynchronous;

d) Device information and status negotiation are transmitted between the devices of the DisPlayport through the auxiliary interface AUX.

3.2 implementation approaches

a) Decoding and receiving of 6 channels of DP video: Supporting 10b/8b decoding and descrambling of the video of one of the 6 channels of DisplayPort, the output is output to the DisplayPort interface.

6-channel DP video encoding and output function: Supports the scrambling of received DisplayPort data and 8b/10b encoding, and outputs to one of the 6-way DisplayPort ports.

Array processing function: After 10b/8b decoding and descrambling of the video of one of the 6-input DisplayPort, after the array is exchanged, the scrambling and 8b/10b encoding are performed, and then output to one of the 6-way DisplayPort ports.

Each of the above functions needs to complete the link establishment of the link between the graphics card and the development board or the link establishment of the development board and the display and the training of the link through AUX.

b) Real-time processing of high-speed physical interface data by high-performance FPGA. This system supports SST 10.8Gbps physical interface, and achieves effective line speed of 8.64 after 10b/8b decoding of 10.8Gbps physical traffic. Gbps to support video streams up to 2560X1440@60Hz. After performing real-time line rate analysis on the video stream, it is mapped into the time slot of the MST and transmitted in the format of MST.

In order to support 2 channels of 2560X1440@60Hz video stream, MST 21.6 Gbps DisplayPort physical interface must be supported. After 10b/8b decoding, the physical interface achieves an effective line rate of 17.28Gbps to support 2 channels of up to 2560X1440@60Hz video stream. Transfer on a DP interface. In order to process and analyze the high throughput with a line rate of 17.28 Gbps, parallel and pipeline processing are used in the design of the FPGA.

In the TX output to the display side, the video stream of up to 2560×1440@60 Hz must be parsed from the time slot of the MST in real time, and converted into the SST format, and then transmitted to the physical interface through 8b/10b encoding.

c) In order to support asynchronous clock processing, the input SST data stream (up to 2560X1440@60Hz video stream) must be parsed and some invalid padding data must be removed in order to transmit data in the MST and at the display according to the TX clock. Adjustment (alignment fill data). In this process, a certain smoothing technique must be adopted to ensure correct resolution of the stream on the receiving side and recovery of the stream clock.

d) Developed the AUX interface protocol; on the RX side, it can respond correctly to the AUX operation of the graphics card; on the TX side, it can correctly read the status of the display, and can tell the current TX operation of the graphics card. Through the AUX interaction, the correct DisplayPort link link is established with the graphics card and display.

4. Summary

This article briefly introduces the basic content of the dp1.2 protocol, and explains how the primary link and the auxiliary link work together. Meanwhile, It has two main functions, the first one is Video cross function, the second one is Multi-stream streaming

Video cross function

The product can realize the cross function of 6 channels of DP 2560 x 1440@60Hz resolution video, and can be arbitrarily crossed by real-time configuration.

Multi-stream streaming

It should be able to implement the multi-video streaming function of the DP v1.2 standard. It can encode two 2560 x 1440@60Hz video streams on one DP v1.2 video channel and can perform reverse processing.

References

[1]. Yucai Yang. DisplayPort Digital Video Design and Research [D]. Hefei University of Technology, 2012.

[2] Jianping Wang. Key Technology and Application Research of DisplayPort Interface [D]. Guilin University of Electronic Technology, 2009.