Research on Fault Diagnosis of Simple Combinational Logic Circuit Based on Virtual Instrument

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Abstract

In the process of the development of electronic circuits, analog circuits sooner than digital circuit occurs, but the development of the digital circuit speed is much higher than analog circuit, the most typical example is the digital computer now has completely replaced the analog computer , rapid development and are still changing. The main reason in addition to military and industrial departments have urgent request for digital system. At the same time, the digital circuit fault diagnosis system of the study have also been placed in the important position. The fault of electronic circuit during application is inevitably. To electronic circuit board in fault, in practice, we always try our best to find where its fault is, and more supply a reference for maintaining later. Aiming at the fault of electronic circuit during application, several kinds of testing are deeply researched in this thesis. Main contents of the thesis are producing algorithm of testing vectors and methods of using fault simulation to judging covering rate of testing vectors in processes of inspecting faults, as well validating testable design of electronic circuit systems. Producing algorithm of testing vectors contains: Pseudo-exhaustive method, D algorithm, Main access sensitizing method, Fault dictionary method.

Keywords

Fault simulation, measurement group generate, D algorithm, LabVIEW programming.

1. Introduction

Circuit fault diagnosis is of great significance in digital circuit design and production process. It helps to repair various defects on the chip template, reconfigure the fault redundancy system, contribute to the improvement of the production process, and analyze the effect of the fault detection method. Etc., ultimately improve the chip's output, quality and reliability. If the existing digital circuit fault diagnosis still relies on conventional instruments and traditional manual analysis, its diagnostic positioning is difficult and the cycle is long, which will seriously slow down the design and production speed of digital circuits. Therefore, the development of digital circuit fault diagnosis system is an effective method to solve the problem of low efficiency of digital circuit fault diagnosis.

With the development of high technology and modern industrial technology, the precision of precision instruments is getting higher and higher, and the system is more and more complicated. The rapid fault detection equipment for electronic systems has been able to locate faults on the circuit board, but at the component level. Circuit board fault detection performance is complicated and complicated, mainly relying on labor. It is difficult to guarantee the quality and efficiency of maintenance by experience. Especially for some complex systems that are put into use soon, due to the relatively few fault statistics and maintenance experience, maintenance support is more difficult. According to the data, the current test cost has reached 50% or even 70% of the cost of the equipment developed. Therefore, it is

necessary to study a component-level circuit diagnostic maintenance system with high versatility and practicability.

The basic idea of digital system fault diagnosis is to load the excitation signal at the input end, get the response at the output end, and determine the fault point according to the combination of excitation and response and the topological relationship of the circuit. The key is the generation of the test vector, that is, what kind of excitation signal is loaded at the input to make the fault point inside the circuit react.

The main problem of this topic is to study the fault test method of digital system, and use fault simulation to test the fault coverage of the vector.

At present, traditional time domain testing and frequency domain testing methods are proven and effective for analog circuits and systems, but they may not work for complex digital circuits and systems, and may even be completely powerless. This is because the information processed by digital circuits and systems is represented by discrete binary information. Therefore, the testing technique for its "data" information in modern digital circuits and systems is called data domain testing technology, referred to as data domain testing.

With the increasing popularity and development of digital integrated circuits and computer technologies, especially the emergence of very large scale integrated circuits, systems in modern advanced equipment are becoming larger and more complex. However, its maintenance and overhaul problems are becoming more and more serious, especially in some real-time controlled online applications, such as aerospace, aviation flight control, weapon system management and control, radar system management and control, and so on. The research content of data domain testing is to study the theory and method of testing and fault diagnosis of digital systems and computer systems.

2. Digital circuit fault diagnosis basics

2.1 Methods and progress in digital circuit fault diagnosis

In 1959, Eldred presented the first test report on combined circuits, which unleashed the prelude to digital circuit fault diagnosis. However, the method proposed by Eldred can only solve the fault test problem of the combined circuit within two levels. Later, DBArmstrong proposed a one-dimensional path sensitization method based on the basic idea of Eldred. The main idea is to find a sensitization path from the fault point to the accessible output for the multi-level gate circuit, so that it can be observed at the reachable end. The fault signal, using this method, solves a considerable number of combined circuit fault detection problems. The Boolean difference calculation method proposed by Yau and Seller, and the Boolean differential algorithm proposed by Thayse, although they have certain difficulties in practical use, they systematically make the theory of path sensitization, so these two theories are in the theory of digital circuit diagnosis. Taking an important position is an important tool and foundation for theoretical research. Subsequently, the well-known D algorithm proposed by Roth theoretically made the combined circuit fault detection and diagnosis reach the highest point.

Roth's D algorithm theoretically solves the problem of combined circuit fault detection and diagnosis, that is, any single fault in any non-redundant combinatorial logic circuit can use D algorithm to find his test vector, but in practical applications, it is calculated. The amount is very large, and it is difficult to implement large-scale complex circuits. In the past, the exhaustive test method, which was considered to have no practical significance, has developed with the increase of circuit scale. The pseudo-poor proposed by Archhambeau et al. in 1984 the test method has opened up a new way to solve the diagnosis problem of large-scale combinatorial logic circuits.

Fault diagnosis of digital circuits includes fault detection and fault location. At present, the main diagnostic methods are: exhaustive test method, pseudo-exhaustive test method, and test code generation method.

1.Exhaustive test method

The exhaustive test method refers to inputting all possible test codes at the input end of the circuit under test to observe whether the circuit output meets certain logic functions.

S is the logic circuit under test, the input vector test code is X, the output vector is Y, and the logic function implemented by circuit S is S, then

$$Y = S（X） \tag{2.1}$$

For any X, there is

$$S*（X）= S（X） \tag{2.2}$$

Then the circuit under test S* becomes fault-free. If there is a group, it makes:

$$S*（X^0）\neq S（X） \tag{2.3}$$

Then the circuit under test S* is said to be faulty. It is called the vector test code for diagnosing this type of fault. The basic idea of the exhaustive test method is that in the n-dimensional Boolean space, there is only one test code, and the test circuit is judged by checking whether the output of the circuit under test meets the pre-specified requirements for each of the test codes. Is there a fault? All faults here are taken into account and the fault detection rate is 100%. However, as the original input dimension n increases, the total number of test vectors increases sharply. When the original input number reaches a certain number, the exhaustive test method for fault diagnosis is unrealistic. A pseudo-exhaustive test method has been proposed for this.

2.Pseudo-exhaustive test method

On the basis of the exhaustive test method, we try to divide the circuit so that each of the divided circuits can perform exhaustive tests, so that the number of tests is greatly reduced, making it practical.

3.Test code generation method

The test code generation method is also to solve the problem that the exhaustive test method has too many test vectors and the test time is too long. The method is to generate a specific test code by a Boolean difference method or a D algorithm for a fault that may exist in the circuit under test, so as to achieve the purpose of fault location.

2.2 Digital circuit fault diagnosis process

The so-called fault is the abnormal phenomenon of any system, so that the system exhibits the undesired characteristics. The fault diagnosis technology mainly includes three steps: fault detection, fault isolation, and fault identification. The so-called fault detection is to judge whether the fault occurs in the system and detect the fault occurrence time; fault isolation is to determine the location and type of the fault after detecting the fault; fault identification refers to determining the fault size and time variation after the fault is separated. characteristic. In essence, fault diagnosis technology is a model classification and identification problem. That is, the operating state of the system is divided into two categories: normal and abnormal. It is a pattern recognition problem to determine which fault signal sample belongs to which fault.

In recent decades, fault diagnosis technology has been extensively studied and many feasible methods have been proposed. Since 1991, IFAC has held a worldwide academic conference on fault diagnosis of control systems every three years. Some well-known automatic control conferences such as ACC and CDC also have fault diagnosis topics, and more and more research papers are available. From the papers published by Isermann and Balle statistics from 1991 to 1995, the fault diagnosis method based on analytical model has been deeply studied, and the combination of neural network and other fault detection methods has gradually increased. Especially in recent years, artificial intelligence fault diagnosis methods have received extensive attention, and a large number of research papers have been published, which has promoted the rapid development of the discipline of fault diagnosis.

3. Acquisition of combinatorial logic circuit fault test set

The combinatorial logic circuit consists of various gate circuits with no feedback connection between the input and output. The output of the combined logic circuit at any time depends only on the state of each input at that time, regardless of the original output state of the circuit. Whether it is an integrated IC chip or a discrete digital circuit, as long as there is a complete fault location test set (a collection of test codes), the circuit fault can be accurately determined. Therefore, the key to the diagnosis of combinatorial logic is to find the fault location test set. Current main diagnostics

The methods are: exhaustive test method, pseudo-exhaustion test method and test code generation method. This topic will use the test code generation method for combinatorial logic circuit fault diagnosis.

The D algorithm is a method of driving the transmission signal successively on the circuit, so that the influence of the fault is expressed at the output end to determine the initial input of the circuit under test, thereby obtaining the test code. The specific idea is to set a fault for a given circuit and add an error signal D to the fault location; find the drive sensitization path of the fault signal D, starting from the set fault location, using bitwise seeking The operation is performed to obtain a path of the error signal D to a detectable output end of the circuit; and then a consistency operation is performed to determine a condition that satisfies each end point of the error signal D drive to obtain a test code.

The D algorithm proposed by Roth has been proved theoretically, and it can find a test set of arbitrary faults for any non-redundant combination circuit. However, in the specific application, because the amount of calculation is too large, especially for large combined circuits, the calculation time is very long, so that it is difficult to put into practical use. The reason for this is that the arbitrariness of the sensitization pathway is too great, especially when considering multi-channel sensitization, the various combinations are too many, but the truly effective combination is often less. In order to reduce the computational workload, the D algorithm can be put into practice, and various improved algorithms are produced. Such as PODEM (Path Oriented Decision Making) algorithm.

The specific practices of the 3.2 NAND gate combination circuit of this subject are as follows.

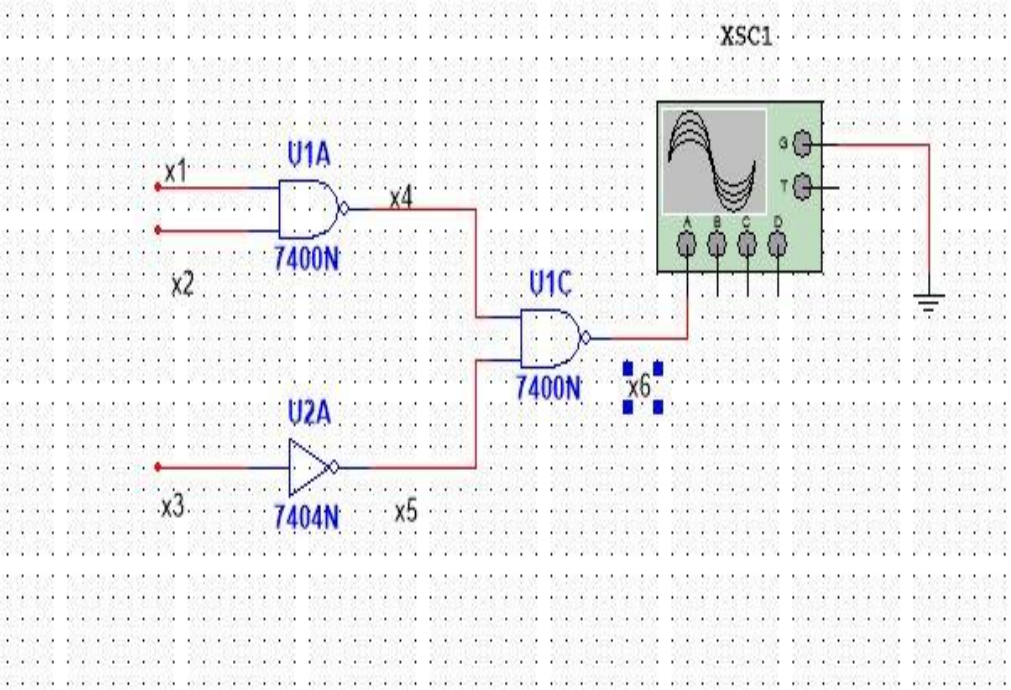

Fig 1.NAND gate combination logic

1. List all fixed faults of the circuit: x1/0, x1/1, x2/0, x2/1, x3/0, x3/1, x4/0, x4/1, x5/0, x5/1,x6/0,x6/1, a total of twelve faults.

2. List the test code for each fault:

Assume that a fault occurs, such as a x4/0 fault in the circuit, ie x4:s-a-0 fault.

①Forward chasing: that is, to find out the condition that x6 takes different values when the fault occurs or does not occur. It can be known from the circuit that when x4/0, x6=1; if there is no x4/0 fault, to make x6=0, x5=1 must be made.

②Reverse chasing: the sensitization path chasing the initial input along the x4 signal transmission in the opposite direction. It can be seen from the circuit that when there is no x4/0 (that is, there is x4=1), x1=1, x2=0; or x1=0, x2=1; or x1=x2=0, both can make x4=1. Thus, three test codes (x1, x2, x3) are obtained: (1, 0, *), (0, 1, *), (0, 0, *). Where * can be either "0" or "1".

③Chasing again: the test code obtained by chasing in the opposite direction often has one or several original inputs that have not yet been decided, and then use the conditions obtained in the positive catch-up to catch up, thereby determining which undetermined initial input values. For this circuit, the undetermined input value is x3=0. The test code to get the catch-up is (*,*,0).

④Combination test code: the test code obtained by the reverse chasing and the test code obtained by chasing it are subjected to bitwise intersection calculation. For this circuit there are:

(1,0,*)Λ(*,*,0)=(1,0,0)

(0,1,*)Λ(*,*,0)=(0,1,0)

(0,0,*)Λ(*,*,0)=(0,0,0)

For the other eleven fixed faults, the same steps can be taken to obtain the respective test codes. See 3.1.

Circuit D algorithm test code table.

Table 3.1 Circuit D algorithm test code table

Serial number	Fault type	Test code（x1 x2 x3）
1	X1/0	（1,1,0）
2	X1/1	（0,1,0）
3	X2/0	（1,1,0）
4	X2/1	（1,0,0）
5	X3/0	（0,1,1）（1,0,1）（0,0,1）
6	X3/1	（0,1,0）（1,0,0）（0,0,0）
7	X4/0	（0,1,0）（1,0,0）（0,0,0）
8	X4/1	（1,1,0）
9	X5/0	（0,1,0）（1,0,0）（0,0,0）
10	X5/1	（0,1,1）（1,0,1）（0,0,1）
11	X6/0	（1,1,1）（1,1,0）（0,1,1）（1,0,1）（0,0,1）
12	X6/1	（0,1,0）（1,0,0）（0,0,0）

3. Acquisition of the minimum complete test set:

Commonly used Boolean difference method, D algorithm and other methods, find the test set of all single faults, then establish a fault table covering all single faults, and then use the "test set implication method" to find the minimum complete test set. Its purpose is to reduce the amount of testing work at the time of diagnosis. The specific method is as follows.

①Number the test code in Table 3.1:

T0=(0,0,0); T1=(0,0,1); T2=(0,1,0); T3=(0,1,1);

T4=(1,0,0); T5=(1,0,1); T6=(1,1,0); T7=(1,1,1).

②Number all faults of the circuit:

F1=x1/1; F2=x2/1; F3=x1/0 or x2/0 or x4/1; F4=x3/0 or x5/1; F5=x6/0; F6=x3/1 or x5/ 0 or x4/0 or x6/1.

③List the diagnosed fault table: The fault table of this circuit is shown in Table 3.2.

Table 3.2 Circuit fault table

Fault number	Fault	Test code and coding	Trouble free output value	Faulty output value
F1	X1/1	T2(0,1,0)	0	1
F2	X2/1	T4(1,0,0)	0	1
F3	X1/0,x2/0,x4/1	T6(1,1,0)	1	0
F4	X5/1 X3/0	T1(0,0,1)	1	0
		T3(0,1,1)	1	0
		T5(1,0,1)	1	0
F5	X6/0	T1(0,0,1)	1	0
		T3(0,1,1)	1	0
		T6(1,1,0)	1	0
		T7(1,1,1)	1	0
F6	X6/1 X4/0 X5/0 X3/1	T0(0,0,0)	0	1
		T0(0,0,0)	0	1
		T2(0,1,0)	0	1
		T4(1,0,0)	0	1

④List the fault coverage table: the fault bar is the upper rail of the table, and the test code Ti is the left column of the table. When Ti can test the Fi, the intersection of the two columns is marked with “#”, which is faulty for this circuit. The coverage table is shown in Table 3.3 Fault Coverage Table.

Table3.3 Fault coverage table

	F1	F2	F3	F4	F5	F6	Trouble free output value
T0						#	0
T1				#	#		1
T2√	*					#	0
T3				#	#		1
T4√		*				#	0
T5				#	#		1
T6√			*		#		1
T7					#		1
cover	√	√	√		√	√	

In Table 3.3, add "√" to T2, T4 and T6. They are the essential test codes: fault F1 can only be measured by T2, fault F2 can only be measured by T4, and fault F3 can only be measured by T6. This single test code that detects a single fault becomes an essential test code. Marked with "*" in the table.

⑤ Select the minimum complete test set: it consists of the essential test code plus the supplemental code.

The minimum complete test set must include the essential test code, because the essential test code can detect a specific fault. For example, the essential test code of this circuit can not only detect F1, F2, F3 faults, but also detect faults of F5 and F6. In the coverage field in Table 2-3, the faults that can be detected by the essence test code are filled in with "√", and only the remaining F4 is not covered by the essence test code as long as the F4 fault test code T1, T3, T5 is detected. Optional one, as a supplemental code, you can get a complete test set of faults: (T1, T2, T4, T6) or (T3, T2, T4, T6) or (T5, T2, T4, T6), 3 tests The set is the smallest and most complete, because any of the three tests can detect all the faults of the circuit shown in Figure 2-1 (F1, F2, F3, F4, F5, F6, F7), no Missing. The number of test codes in the minimum complete test set can no longer be less, otherwise the fault will be missed.

4. Fault Diagnosis of Combinational Logic Circuit Based on LabVIEW

In the previous chapter, the minimum test set for faults in the circuit has been derived. By using four test codes for cross-test, all faults can be accurately determined. From the three minimum test sets: (T1, T2, T4, T6), (T3, T2, T4, T6), (T5, T2, T4, T6), one of the minimum test sets for final use, this paper Select (T1, T2, T4, T6) as the final test set. Then list Table 4.1:

Table 4.1 Minimum test set fault output table 1.

Fault number	Fault	Test code and code	No fault output value	Fault output value
F1	X1/1	T1(0,0,1)	1	1
		T2(0,1,0)	0	1
		T4(1,0,0)	0	1
		T6(1,1,0)	1	1
F2	X2/1	T1(0,0,1)	1	1
		T2(0,1,0)	0	0
		T4(1,0,0)	0	1
		T6(1,1,0)	1	1
F3	X1/0 X2/0 X4/1	T1(0,0,1)	1	1
		T2(0,1,0)	0	0
		T4(1,0,0)	0	0
		T6(1,1,0)	1	0
F4	X5/1 X3/0	T1(0,0,1)	1	0
		T2(0,1,0)	0	0
		T4(1,0,0)	0	0
		T6(1,1,0)	1	1
F5	X6/0	T1(0,0,1)	0	0
		T2(0,1,0)	0	0
		T4(1,0,0)	0	0
		T6(1,1,0)	1	0
F6	X6/1 X4/0 X5/0 X3/1	T1(0,0,1)	1	1
		T2(0,1,0)	0	1
		T4(1,0,0)	0	1
		T6(1,1,0)	1	1

Front panel design

Place a minimum test set on the left front panel. There are three minimum test sets. This paper has been introduced in Chapter 3 and will not be described here. Finally, the test set (T1, T2, T4, T6) was selected as the minimum test set of inputs, which are (0 0 1), (0 1 0), (1 0 0), (1 1 0), input minimum

test. Set the function area; one test set has four test codes, the test code area is the test set displayed in the current input circuit; the value area shows the number of the test code currently input in the test set.

In the middle is the digital circuit diagram to be tested.

The output area on the right side is set for the test code input area. It displays the corresponding circuit output value when a certain test code is input. After the four test codes are completely input, the four output outputs are completed, and the output is accumulated. In the output array area, form an array. According to the output array, the specific fault of the digital circuit can be judged according to the following fault comparison table.

2. Program drawing

(1) Index of the array: The minimum test set is an array of four rows and three columns. In order to achieve the purpose of detection, four arrays need to be sequentially input into the circuit. After the array is created, connect it to three two-dimensional array indexes, and connect 0, 1, and 2 on the column index of the three array indexes, that is, input all the three columns of each row into the circuit; connect the loop count to The row of the array index is therefore counted by the for loop to ensure that all four lines of test code are input into the circuit.

(2) Circuit input and output: After adding the above input to the circuit, an output control is established, corresponding to the output area of the front panel. Finally, an array generation control is added to the for loop to display the last output array.

Add a time delay to the for loop with a delay of 1 second, so that the final result is output sequentially.

5. Conclusion

The key and difficult point of digital circuit fault diagnosis is test generation. Boolean difference method is an important algorithm for generating test vector of combined circuits. Its description is strict and concise, and its physical meaning is clear. It plays an important role in the diagnosis theory of digital systems. However, since solving the Boolean difference requires a large number of XOR operations, especially the solution of the high-order Boolean difference is very cumbersome, which makes it difficult to use in practical use. Therefore, the research on the test generation of combinatorial logic circuits mainly focuses on the research of search algorithms. On the basis of the D algorithm, PODEM algorithm, FAN algorithm, SOCRATES algorithm, EST algorithm, etc. have appeared successively. These are gate-level algorithms, which can be used for fault diagnosis of combined circuits. This article is a simple combination circuit fault diagnosis, using the D algorithm can basically solve all faults.

In this paper, the D algorithm is used to obtain the fault test code through the circuit, and the test code combination can be selected by testing the circuit properties to form the minimum test set. All of this is achieved by using Multisim for digital circuit simulation.

In this paper, LabVIEW programming is used to detect faults. According to the above data, cyclic input, cumulative output, and arrays are compared with the prepared fault table to reduce the inconvenience of full manual search and realize automatic fault finding.

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