A high-precision programmable signal generator with self-calibration function

Bilu Luo

China electronics technology corporation 36 institute of technology, Zhejiang 314033, China

Abstract

With the development of electronic equipment, a better precision of signal generator is needed for testing high precision electronic equipment. The signal quality of traditional signal generator, especially for the type of analog oscillation, is susceptible to environmental factors, and the frequency reference source has some drift, which needs to be calibrated periodically. In this paper, a high-precision programmable signal generator with self-calibration function is designed for the defects of the existing signal generator which can't satisfy the high accuracy signal in the extreme environment, and the frequency accuracy was better than 0.5%.

Keywords

self-calibration, feedback, frequency accuracy.

1. Introduction

Signal generator is a kind of equipment which can provide various waveforms to the outside world and is used as a test or excitation device [1, 2]. With the rapid development of electronic technology, the high performance signal generator is urgently needed. The signal generator can be divided into analog and digital types according to working principle: The reference frequency of analog signal generator is generated by the oscillator circuit, and the phase and frequency are adjusted by means of simulation [3]. Digital signal generator can make use of full digital technology to synthesize the benchmark clock. The internal circuits of traditional signal generator are easily influenced by environmental factors, and the frequency accuracy of signal generator is influenced by factors such as temperature drift and ageing drift [4, 5]. This article, based on a FPGA + DSP architecture of digital processing platform and take advantage of low noise, high resolution DAC(digital to analog converter) and ADC(analog to digital converter) chip, to design an automatic calibration function of high precision programmable signal generator. The test results indicate that the output bandwidth of the signal generator designed in this paper is 0.5 Hz-20MHz, and the waveform is less than 2 μs, and the frequency accuracy is better than 0.5%.

2. Basic principles and hardware architecture

The hardware platform of programmable self-calibration signal generator is shown in figure 1, which consists of power supply module, FPGA, DSP, DAC, ADC, DDR, Flash, touch screen, etc. FPGA achieves the control of each function, DDR for data caching, and DAC is used to output various waveforms, ADC for convert the analog amount of the feedback signal into digital quantities, DSP for calculating the deviation of the output voltage and to obtain the compensation voltage.

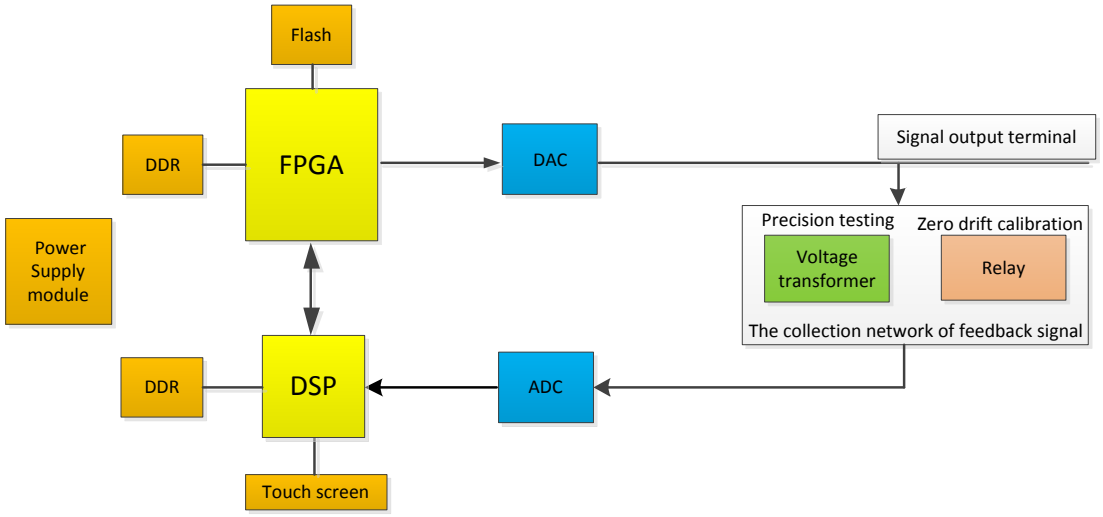

Fig. 1 The hardware platform of programmable self-calibration signal generator

2.1 The realization of self-calibration circuit

The automatic calibration function of programmable self-calibration signal generator is realized by the feedback loop in the circuit. Feedback signal collection network, ADC, DSP, ADC, DSP, FPGA and DAC form the feedback loop. Its working mechanism is as follows.

The feedback loop is mainly composed of feedback signal acquisition network, high precision ADC and a single DSP. The feedback signal acquisition network includes two different channels for zero drift calibration and precision monitoring. Zero drift calibration is mainly used to calibrate the zero voltage when the machine is switched on. The internal specific workflow is: At the beginning, click the "zero drift calibration" option on the touch screen, and the DSP sends the received instructions to the FPGA, when the FPGA enters a zero-value encoding to the DAC. Then, FPGA sends the instructions to the sampling module of the feedback signal. The relay switches to the zero-drift calibration channel and then converts the collected feedback signal into DSP after converting it into a digital signal. Based on the Fourier transform DSP algorithm, the base wavelength of the feedback signal is used as the final zero drift input FPGA. Finally, the FPGA sends the corresponding compensation code to the DAC module based on the zero drift value. As in the above circular compensation, until the zero drift value is less than 5mV, and the zero drift calibration factor is stored in Flash, the correlation coefficient can be automatically loaded at the next startup.

The operation mechanism of the real-time precision detection channel is similar to the zero-drift channel. The collected feedback signal needs to be converted into a signal within the range of ADC range by a voltage transformer. When the feedback loop detects that the output voltage is better than 0.5%, it stops the automatic calibration function and controls the output signal of the signal output.

2.2 Digital to analog conversion module

The DAC chip is the core component of the waveform, which is designed with 18 voltage output DAC chips AD5780. This DAC has the advantages of high precision, short time and low noise. The relative accuracy of this DAC is ±1 LSB, and the maximum value of differential nonlinearity (DNL) is ±1 LSB, which can meet the design requirements. The DAC output waveform is referenced by reference voltage, so the reference voltage accuracy is extremely high. The design adopts high accuracy and low temperature drift reference voltage source ADR445 to provide reference level to AD5780, and its output typical output noise is only 2.25 μV.

2.3 Analog to digital conversion module

ADC chip is used for real-time monitoring of the output voltage accuracy and the initial zero drift of the equipment, so the accuracy performance of ADC circuit directly affects the accuracy of the signal. The output voltage range of the programmable self-calibration signal generator is larger, so a voltage

transformer is needed to reduce the voltage amplitude detected to the range of the module conversion chip. Based on the characteristics of small amplitude and low frequency of sampling feedback voltage, this design adopts the low sampling rate and high resolution characteristics of the 24 bit ADC chip AD7765 produced by ADI. The feedback voltage of the signal generator is a single terminal voltage, and when the amplitude of the output signal is small, the feedback signal of it will be interfered by the noise, so that the feedback loop can produce a larger measurement error. Therefore, this paper converts single - end feedback signal into differential signal, which can effectively inhibit the interference of common mode noise to small signal. The differential amplifier circuit in figure 2 converts the feedback signal collection network output into a single - end signal into a differential signal.

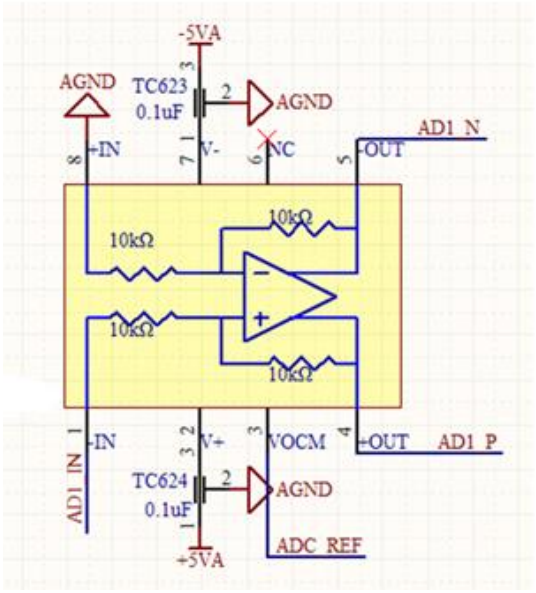

Fig. 2 Circuit diagram of differential amplifier

The input of the amplifier is connected with the feedback signal, the other end is grounded, the output end is the differential signal, and the equivalent circuit model is shown in figure 3

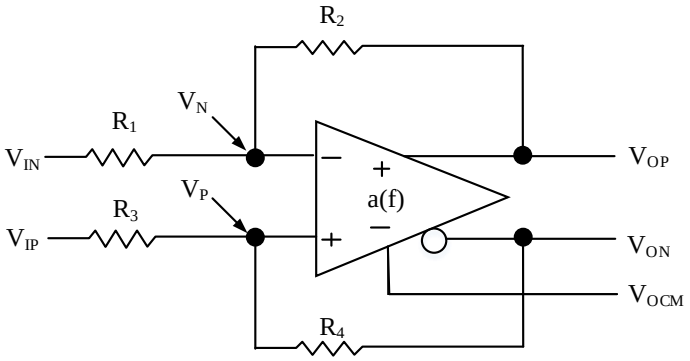

Fig. 3 The equivalent circuit model of differential amplifier

Above, V_{IN} as the feedback signal, power amplifier input node to V_a, V_b, amplifier output voltage V_1, V_2, for the convenience of analysis, makes the open loop gain of the amplifier is equal to A_0, then can get the voltage equation below.

$$V_1 - V_2 = A_0 (V_b - V_a) \tag{1}$$

For $B_1 = R_3 / (R_3 + R_4)$, $B_2 = R_1 / (R_1 + R_2)$, the differential closed-loop gain of the amplifier is calculated according to the basic characteristics of the ideal model of the integrated amplifier.

$$A_{DD} = \frac{2 - B_1 - B_2}{B_1 + B_2} \tag{2}$$

The common mode rejection ratio is

$$CMRR = \frac{A_{DD}}{A_{DC}} = \frac{2 - B_1 - B_2}{2(B_2 - B_1)} \quad (3)$$

According to formula (2) and (3), the accuracy of the closed-loop gain of the differential amplifier circuit and the common mode rejection ratio depend on the matching degree of the feedback resistance. This design adopts the form of adjustable small resistance, which makes the closed-loop gain of the differential amplification circuit less than 2%, and CMRR less than 90dB.

2.4 Design of core digital processing circuit

This design adopts Xilinx's FPGA chip XC5VSX95T to control the function modules of DAC, ADC and calibration, and to complete the information interaction with DSP. XC5VSX95T adopts the second generation advanced chip column architecture, which has a large number of built-in IP hard core system, which can be directly used in the control program of this design, greatly reducing the FPGA programming cycle. The FPGA is external to a 1Gb DDR3 chip. And a 32MB FLASH to support the initialization and calibration of information storage.

DSP, as a high performance computing processor, is suitable for real-time processing of feedback data of signal generator. The design uses TI's multi-core DSP TMS320C667, which contains eight 1.25GHz cores and all of eight cores to share storage, supporting various high-speed external interfaces such as SRIO, PCIe and Gigabit. DSP mainly realizes the functions of feedback signal acquisition, data processing and LCD touch screen control. Using CCS V5 to complete the editing and debugging of software, DSP software flowchart is shown in figure 4

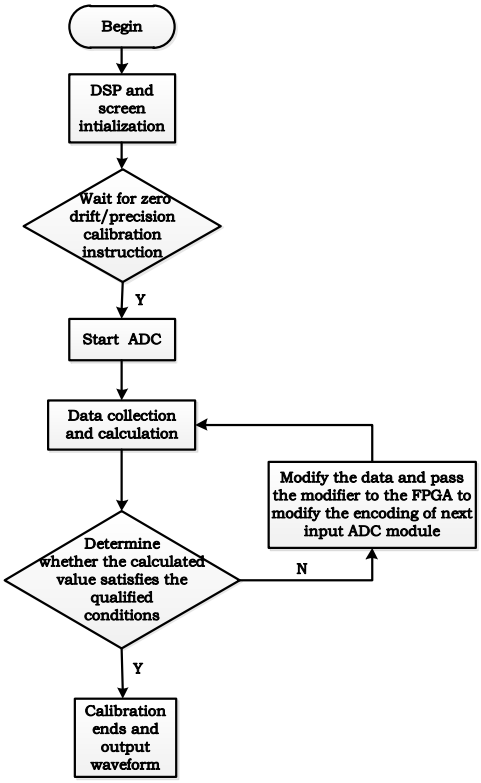

Fig. 4 The software flowchart of DSP

3. Performance of the signal generator and test

3.1 Main functions and performance indicators

This paper designed the signal generator is mainly used to produce low frequency sine wave, square wave and other commonly used test signal, the user can also through the liquid crystal display interface, by setting the parameters of the system to provide, custom output waveform. In addition, the signal

generator provides a USB interface to support the PC terminal interconnection, and the advanced setting of data interaction and input waveform. The main properties of the signal generator designed in this paper include

(1) Bandwidth 0.5 hz-20mhz
(2) The maximum output voltage is plus or minus 15V
(3) Output signal resolution 18bit
(4) Frequency accuracy 0.5%
(5) Signal setting time ≤2μs

3.2 Test of output waveform

The test conditions of the system are based on the high sampling rate oscilloscope HDO6000 of Teledyne Leroy. The bandwidth of this oscilloscope can be up to 1GHz, with a resolution of 12bit, which meets the requirements of the output waveform test. According to the main performance of the signal generator, the sine wave and the square wave pulse signal are tested. The frequency accuracy of the signal generator is better than 0.5% by measuring the output sine waves which have the amplitude of 5V and the frequency respectively 0.5 Hz, 20Hz, 2KHz, 200KHz and 200MHz. The specific test results are shown in table 1

Table 1. Test results of frequency accuracy

setting frequency(Hz)	0.5	20	2K	200K	20M
actual frequency(Hz)	0.500	19.982	1.995K	199.314K	19.916M
Frequency accuracy	0%	0.09%	0.21%	0.35%	0.42%

Using the oscilloscope to test the square wave of 1KHz, as shown in figure 5, the time of establishment of the measured waveform is 1.82 μs.

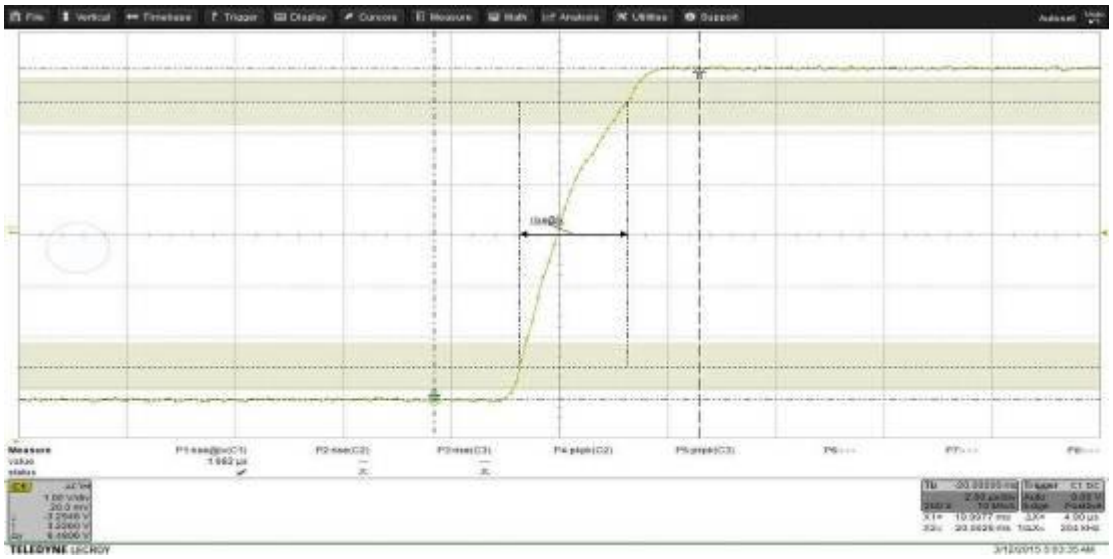

Fig. 5 The rise time of the square wave with 1KHz frequency

4. Conclusion

The signal generator introduced in this paper can output bandwidth of 0.5 hz-20mhz according to the user's demand. Its maximum advantage is the feedback loop composed of high precision ADC and DSP, which solves the defects of the traditional signal generator frequency accuracy due to the influence of the external environment. It can satisfy the requirement of high precision waveform when it can meet the test in bad environment. In addition, the signal generator can be expanded to multichannel output by increasing the number of ADC chips.

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