FPGA Implementation of Background ADC Calibration in Digital Domain

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Abstract

The signed variable step size least mean square (SVSS-LMS) algorithm which is used for digital background calibration of the pipelined analog-to-digital converters (ADC) is proposed. It is capable of calibrating the most known errors, including finite op-amp gain, capacitor mismatch and comparator offset. The variable step size u is verified with MATLAB. And then, the hardware implementation in Xilinx FPGA device is discussed. The simulation results show that with the proposed SVSS-LMS calibration algorithm, the pipelined ADC can achieve a DNL of -0.59/0.28 LSB, an INL of -0.59/0.28 LSB and SFDR of 82.77dB at input near Nyquist frequency of 41.56MHz.

Keywords

Pipelined ADC; Background calibration; signed variable step size; FPGA.

1. Introduction

Pipelined analog-to-digital converters (ADCs) are a popular choice in high-speed, high-resolution, low-power applications, and it gradually becomes a research hotpot. It has important applications in many fields, such as medical image equipment, radar, etc. The ADC is the key of digital processing system [1-3]. In order to improve the performance of pipelined ADC, digital assisting circuits can be requisite. The digitally-assisted ADC is designed to reduce the analog limitation of ADC.

In nowadays, various calibration techniques have been proposed. They organized in two major categories: foreground and background calibration. The former has the advantage of fast convergence. But there are two drawbacks existed. One is that it can't follow the tracks of errors. The other is that it interrupts regular ADC process. In contrary, background calibration work online during conversion [4]. This property allows continuous system monitoring without interruption and enables tracking of slow environmental variations which caused by PVT (temperature, supply voltage and device aging) [5].

This paper exploits equalization-based background calibration technique, with the help of a slow but accurate ADC in parallel[6]. The gradient algorithm is used to estimate the tap weight values which are unknown due to system errors. By using signed variable step size LMS (SVSS-LMS) this method can be further enhanced. Compared to variable step size (VSS) and modified variable step size (MVSS) approaches, SVSS technique can follow the varying errors with low complexity and low power consumption, and speed up the convergence [7].

In this paper, SVSS-LMS technique is implemented on FPGA, and applied to a 12-bit pipelined ADC which composed of nine 1.5-bit stages and a 3-bit flash. The technique aims to calibrate the errors, including capacitor mismatch, comparator offset and both linear and nonlinear OpAmp imperfection. The advantage of this technique is that it consumes less power in analog circuits, especially in the reference ADC. Furthermore, the fast convergence reduces the time required for the testing done at the production-line. Therefore, the fast calibration techniques increase production throughput and revenue.

The rest of the paper is organized as follows. In section II, a digital calibration based on equalization is presented. Calibration Algorithm and System Architecture is explained in section III. The simulation results are discussed in section IV. Finally some conclusions are provided in section V.

2. Pipliened Adc Structure And Modelling

As shown in Figure 1, the structure of the pipelined ADC consists of N stages, which using 1.5bit/stage architecture, with the last stage is a flash ADC. And the structure of the stage1 is composed of: sample and hold circuit, sub-ADC, sub-DAC, sub-tractor and inter-stage amplifier. Next, the nonlinear transfer function of a 1.5-b/stage is expressed.

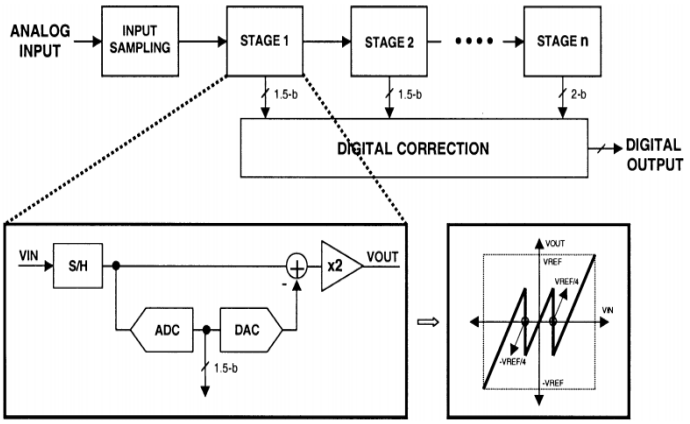


Figure.1. Pipelined ADC 1.5bit/stage architecture

As Fig.2 shows that a typical switched-capacitor 1.5-b pipelined ADC stage, the residue voltage can be expressed as:

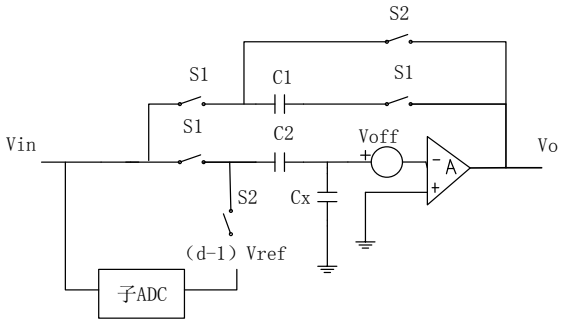


Fig.2 1.5-bit/stage architecture

Assume the open-loop input-output static characteristic of the opamp can be illustrated in the following polynomial equation :

$$V_o \approx \alpha_1 V_\chi + \alpha_2 V_\chi^2 + \alpha_3 V_\chi^3 \tag{1}$$

If the opamp is placed in a feedback circuit, the input (Vx) can be approximated by:

$$V_\chi \approx \varepsilon_1 V_o + \varepsilon_2 V_o^2 + \varepsilon_3 V_o^3 \tag{2}$$

Where, $\varepsilon_1 = \frac{1}{\alpha_1}$, $\varepsilon_2 = \frac{-\alpha_2}{\alpha_1^3}$, and $\varepsilon_3 = \frac{2\alpha_2^2 - \alpha_1\alpha_3}{\alpha_1^5}$.

With applying the above equations, the MDAC transfer function can be shown:

$$V_o = \frac{(C_1 + C_2)V_{in} - C_2(d-1)V_{ref} + (C_1 + C_2 + C_x)V_{off}}{C_1 + \frac{(C_1 + C_2 + C_x)}{A(V_o)}} \tag{3}$$

where, V_{ref} is the reference voltage, V_{off} is the offset voltage, Vo is the nonlinear OpAmp gain, Cx is the parasitic capacitance, C1 is the feedback capacitor, C2 is the sampling capacitor. d is the sub-ADC

output of the current stage that assumes a value of 0, 1, or 2. After dividing (3) by Vref , a digital equation is obtained,

$$D_i(\frac{C_1+C_2}{C_1}) = D_o(1+\frac{C_1+C_2+C_x}{C_1}\cdot\frac{1}{A(D_o)}) + (d-1)(\frac{C_2}{C_1}) - D_{off}(\frac{C_1+C_2+C_x}{C_1}) \quad (4)$$

where $D_i = \frac{V_{in}}{V_{ref}}, D_o = \frac{V_o}{V_{ref}}, D_{off} = \frac{V_{off}}{V_{ref}}$. Using (4) the I-O relation of single stage pipelined ADC can be approximated by:

$$D_i = \alpha_1 D_o + \alpha_2 D^2_o + \alpha_3 D^3_o + \beta(d-1) - \gamma D_{off} \quad (5)$$

Where, $\alpha_k = f_k(C_1, C_2, C_x, A(D_o))$, $\beta = \frac{C_2}{(C_1+C_2)}$, $\gamma = \frac{C_1+C_2+C_x}{C_1+C_2}$. Since $D_{o,N} = D_{i,N+1}$, for the Nth stage in pipelined ADC, therefore, the input for multi-stage as follows:

$$D_i = \alpha_{1,1} D_{i,2} + \alpha_{1,2} D^2_{i,2} + \alpha_{1,3} D^3_{i,2} + \beta_1(d-1) - \gamma_1 D_{off} \quad (6)$$

Where, $D_{i,2}$ is obtained from previous stages, (6) can be expand as:

$$D_{i,N} = \alpha_{N,1} D_{i,N+1} + \alpha_{N,2} D^2_{i,N+1} + \alpha_{N,3} D^3_{i,N+1} + \beta_N(d-1) - \gamma_N D_{off} \quad (7)$$

Eq. (7) shows that Di is calculated beginning from backend stages to reach front stages. Similarly, the calibration technique will be presented in the next section.

3. Lms Variable Step Size Algorithm

As mentioned earlier, the redundancy between pipelined stages is utilized at the proposed calibration technique, aims to correct the final ADC output. Fig.3 shows a 12-bit pipelined ADC which used to correct the errors with the technique.

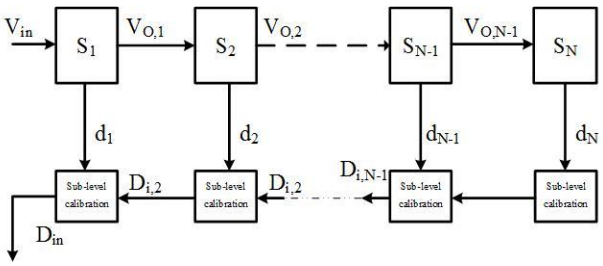


Fig. 3 Reverse pipelining of the multistage adaptive digital filter

3.1 LMS Based Adaptation Technique

In the work, only the first four stages are calibrated for targeted accuracy. For the first two stages, a 5-tap ADF is implemented, and the other stages only two taps per stage are necessary as pointed out in (6).The equation of the weight update based on LMS as follows:

$$w(n+1) = w(n) + \mu(n)e(n)D_{i,N+1}(n) \quad (8)$$

3.2 SVSS-LMS Based Adaptation Technique

The proposed technique uses SVSS algorithm to reach low misadjustment with fast convergence rate.The algorithm is signed variable step size, where its step size using the sign of the error as follows:

$$\mu(n+1) = \theta\mu(n) + \rho sign(e(n)) \quad (9)$$

Where θ is a constant called forgetting factor, and ρ is constant range from 0 to 1. The step size μ(n) changes every iteration according to:

$$\mu(n) = \begin{cases} \mu_{max} & if\ \mu(n+1) > \mu_{max} \\ \mu_{min} & if\ \mu(n+1) < \mu_{min} \\ \mu(n+1) & otherwise \end{cases} \quad (10)$$

And the initial step size is set to μ_{max} that depends on the maximum eigen value presented by:

$$0 < E\{\mu_{max}\} < \frac{2}{\lambda_{max}} \quad (11)$$

When the ADC error grows, the $\mu(n+1)$ is small to quicken convergence. When the ADC error becomes small, the $\mu(n+1)$ changes little bigger to improve accuracy.

4. Simulation Results And Disussion

The previously mentioned algorithms are implemented in Fig.5. The SVSS parameters are set to θ=0.996 ， and ρ=1e-6. The MSE (mean square errors) curves are obtained for each algorithm using input sine wave with frequency 43.97MHz. It can be shown that the SVSS algorithm reach -75 dB which is iteration number about 300. On the other hand, the FSS reaches the same steady state at iteration number about 800. The SVSS algorithm proves to have great convergence curve.

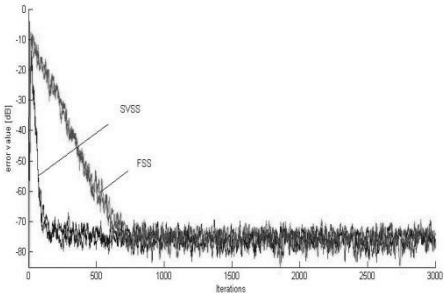


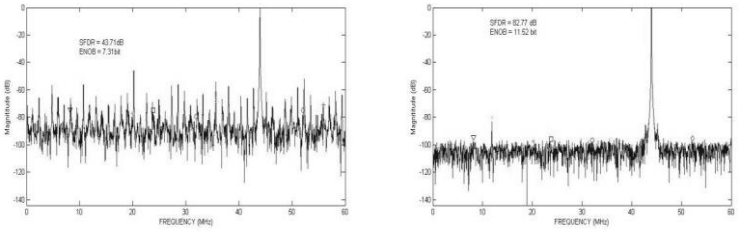
Fig. 4 Learning curve of FSS vs SVSS

Then this proposed algorithm has been verified by implementation using Xilinx FPGA Virtex-5. OpAmp nonlinearities up to the 3rd order besides linear errors including finite gain, capacitor mismatch, parasitic capacitor and comparator offset are corrected in the first two stages. The parameters are shown in table I:

Table 1 Error Parameters Of The ADC

Pipeline stage	Op-amp DC gain	Capacitor mismatc	Comparator offset
1-2	53dB	20%	0.2Vref
4-9	55dB	10%	0.1Vref

Fig.6 shows the dynamic performances before calibration and after calibration. Fig.6 gives the performance before calibration, and Fig.7 gives the calibrated static performance with the proposed algorithm. With the input signal at 41.56 MHz, the SFDR has been improved from 43.63to 81.66dB, the ENOB has been increased from 7.31 to 11.12. The DNL was respectively improved from -1/+4.1LSB to -1/+0.93 LSB, and the INL was improved from -60.47/+61.32 LSB to -0.98/+0.97 LSB.



(b)

Fig.5 Frequency spectrum for (a) before calibration
(b) after calibration

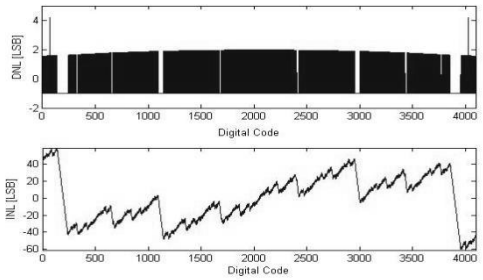


Fig.6 DNL and INL before calibration

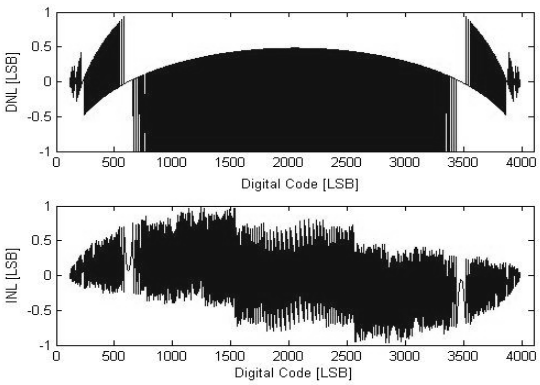


Fig.7 DNL and INL after calibration

5. Conclusion

This paper investigated a digital calibration using SVSS-LMS algorithm. This proposed algorithm has been verified by FPGA implementation employing Xilinx FPGA XC5VFX70t-1ff1136.this proposed algorithm improves the error tolerant capability and speed up the convergence. Verified on FPGA shows it increases ENOB from 7.1b to 11.52b, SFDR from 43.71dB to 82.77dB. Moreover, the convergence time has been reduced, which is only 25% of that in[7].

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