Design of Vernier Delay Loop Time-to-Digital converter with 0.18um CMOS technology

Wei Wang [a], Yongchun He [b] and Mengjia Huang [c]

School of Posts and Telecommunications, Chongqing University, Chongqing, 400065, China;

[a]935549301@qq.com, [b]1149443231@qq.com, [c]260969133@qq.com

Abstract

This paper presents a time-to-digital converter (TDC) architecture with wiener delay ring capable of reaching high-precision and high-linearity based on 0.18um CMOS technology. To design this TDC, it uses a novel coarse counter which is made of a ring of transmission delay architecture, what's more, it also employs interpolation and wiener technology. Interpolator is composed of a coarse interpolator & synchronizer and a fine interpolator based on a single–stage wiener delay loop. Under the working voltage of 1.8 V, the TDC reaches a dynamic range of 208ns, 10ps resolution and the effective precision better than 11ps. The differential non-linearity is -0.2LSB<DNL<0.2LSB. The integral non-linearity is -0.3LSB<INL<0.3LSB.

Keywords

The time-to-digital converte, The coarse counter, The coarse-fine synchronizer, The fine interpolator.

1. Introduction

Time to digital converter (TDC) is a kind of common circuit of time measuring, counting main reference signal to the event happened time is the time interval between two pulses, the time interval of directly into the high accuracy of numerical value.Time to digital converter is widely used, such as scientific experiment [1], [2] a measuring instrument, positron imaging [3], biomedical [4], etc., has the very high precision.

There are two kinds of time to digital converter is implemented: one is based on FPGA is half a custom [5], [6], the other is based on CMOS full custom [7], [8].Half a custom design based on FPGA is a kind of the most flexibility, short development cycle, lower development costs, most suitable for small batch, many kinds of applications, but is limited by the hardware conditions, normally only USES the limited number of structure.Based on CMOS and full custom method is time-consuming and high cost of shortcomings, but for the designer, the design flexible, and performance is the best, is the most active field in the study of TDC.

Now put forward many kinds of time full custom method based on CMOS digital converter to improve the resolution and dynamic range, such as pulse deflating TDC [7], the gating ring shock TDC (GRO) [8], local interpolation TDC [10], delay line/ring, wiener delay line/ring, etc.They can reach several hundred, the resolution of a few decades, more than ten seconds, even some can reach a few picoseconds.In the literature [7], using pulse shrinkage method, resolution of 40 ps, integral nonlinear for LSB 0.6 mm.The method of literature [8] with ring oscillator, make the precision of the TDC 4.2 ps, INL for ps 4.5 mm.Literature [10] to use interpolation techniques, a clock cycle into 992 pieces and make the resolution of about 10 seconds, accuracy of 17.2 seconds, the dynamic range of 160 nanoseconds.

high resolution, high dynamic range, and good linearity.Structure of this paper are arranged as following: the second part of the overall structure of the TDC is designed, the third part of the circuit of each module, the fourth part is the results of simulation analysis, the fifth is the summary of the points on the design structure of TDC.

If need high resolution and large dynamic range at the same time, will be introduced interpolation technology, this paper adopted the coarse count and interpolation method of combining the two.Rough counting USES a new type of structure of propagation delay, interpolator points of coarse and fine, fine interpolator is based on the ChanJie wiener delay ring structure [10], not only has the characteristics of high resolution, high dynamic range, and good linearity.Structure of this paper are arranged as following: the second part of the overall structure of the TDC is designed, the third part of the circuit of each module, the fourth part is the results of simulation analysis, the fifth is the summary of the points on the design structure of TDC.

2. TDC circuit integral structure design

2.1 wiener delay line working principle of the TDC

Figure 1 is the basic structure of wiener delay line TDC, adopted two delay line, two delay line due to the propagation speed, the transmission speed, a slow speed, hence the propagation time difference.Two lines per level unit delay propagation delay delay line of TS and TF, respectively, the TS > TF.Wiener delay line resolution TDC is the delay time, the two delay chain can be represented as:

$$R=T_S-T_F \tag{1}$$

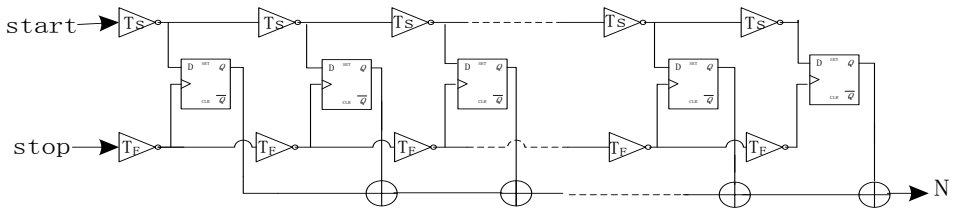

Fig. 1 Wiener delay-line TDC

Input the STOP signal in the chain of wiener conerted to lag behind the rapid spread of signals in advance to catch the spread of the slow START.When the STOP signal pursued to with a START signal phase at the same time, can through the state of the trigger output code how many level forward after the START, the STOP signal measurement of two interval can be represented as:

$$T=N*(T_S-T_F) \tag{2}$$

Because of the two lines of work environment, when the environment changes, two lines will change the same Δ, after subtracting the there is no change, so the environment will have little impact on the type wiener TDC.Thus it can be seen in the different environment to measure the change is not large, can improve the accuracy of measurement.

2.2 TDC 'integral structure design

In this paper, the structure of TDC is the combination of rough counting and two level interpolation.The use of coarse count can make dynamic range is very large, as long as there is enough space to store data counter.The interpolation points of coarse and fine, fine interpolator is composed, ChanJie wiener ring has high stability, the characteristics of high resolution.Figure 2 is the overall structure of the TDC design, structure, six counter by transmission delay, coarse interpolation & synchronizer and fine interpolation based on ChanJie wiener ring device.

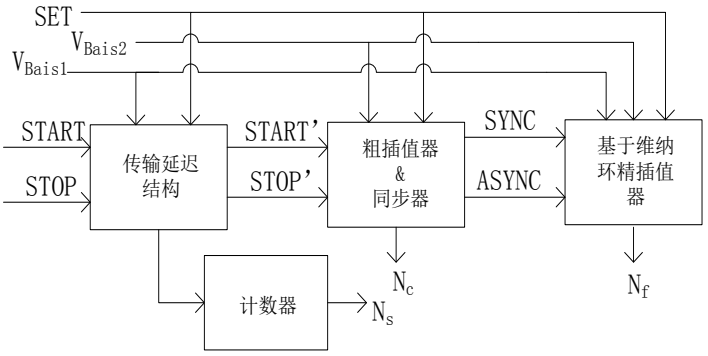

Fig. 2 TDC structure as a whole

Transmission delay structure can produce periodic oscillation signal Ts;Counter is a six addition, every rise along just count once;Coarse interpolation apparatus & transmitting delay structure of synchronizer of a periodic signal processing, after the first will arrive STOP 'and then START' rising along the location represented by encoder Nc, then the two signal is obtained by synchronizer extract SYNC and ASYNC two signals;Fine interpolator used ChanJie wiener ring structure, overtake ASYNC until the SYNC signal, the TDC finish work.

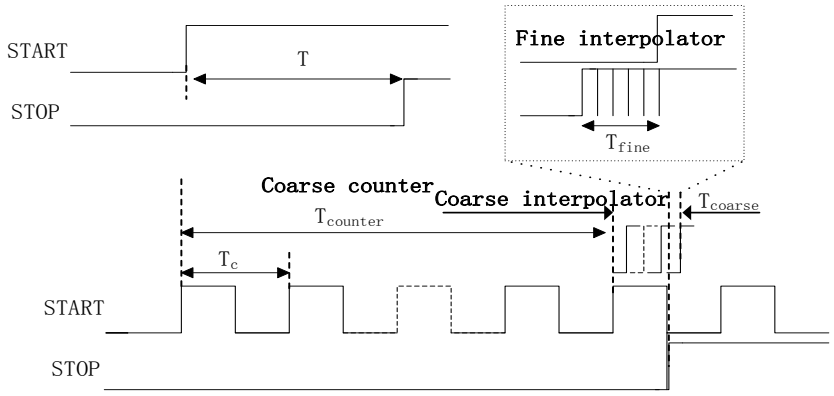

Fig. 3 Working principle of the TDC

Figure 3 is the working principle of TDC, as can be seen from the diagram TDC measuring the time interval can be expressed as:

$$T=T_{counter}+T_{coarse}-T_{fine} \quad (3)$$

$T_{counter}$ began to STOP the spread of the signals the end of the START signal integer delay time of periodic signal, T_{coarse} is coarse interpolation of measuring results, T_{fine} was pure interpolator measurements.

3. TDC key module circuit design

3.1 Voltage-controlled delay unitwiener

Voltage-controlled delay unit structure as shown in figure 4, is composed of two inverter, its propagation delay changes done by NMOS tube under the control of charge and discharge, with him instead of inverter, the performance is very stable, and he - voltage delay linearity is very good, can be seen from the figure 5 is.Figure 5 is a voltage-controlled delay unit at 10 ℃, 27 ℃ and 40 ℃ the three temperature, delay time changes over the control voltage graph, between 1 V - 1.5 V has the very good linearity.Also can be seen from the picture with the temperature change delay unit under two different control voltage delay time basic remains the same, so can reduce the temperature on the influence of fine interpolator based on wiener ring.

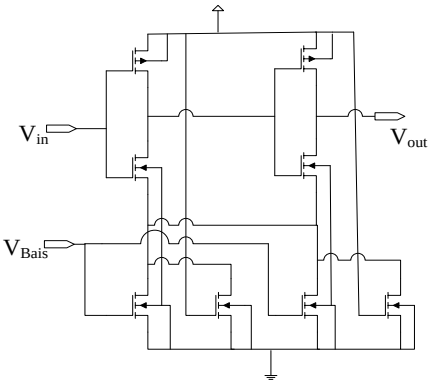

Fig. 4 Delay unit

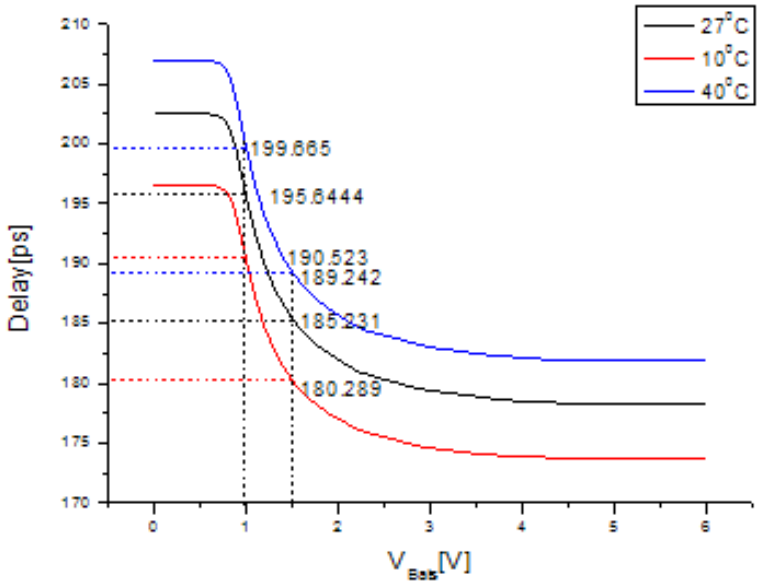

Fig. 5 Delay - voltage under different temperature simulation figure

3.2 Transmission delay structure.

In order to get long time dynamic range and high resolution digital converter, this article adopts the method of coarse count plus interpolator.Actually interpolation technology, there are two ways: one is the START signal and the reference clock signal synchronization, this situation is just a set of interpolator to measure to reach the STOP signal and was followed by a clock rise along the time interval between;Another kind is the START and STOP signals and the reference clock signal asynchronous, this kind of situation need to two sets of interpolator for interpolation process START and STOP signals respectively.Now many people focus on the second approach, although he wants to use two sets of interpolation counters, because of the randomness of the START signal, it is not easy to START signal and clock synchronization.In order to synchronize the signal, so in the transmission delay is proposed in this paper a new type of structure, you can generate a clock cycle is 3.3 ns periodic oscillation signals.

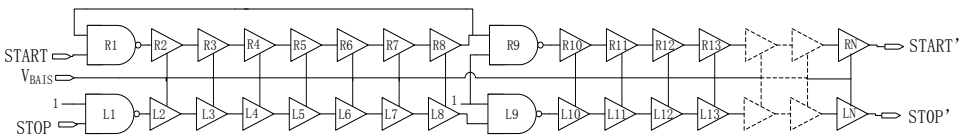

Fig. 6 Transmission delay structure

Figure 6 is the transmission delay of the circuit structure, the START signal transmission to delay ring, the STOP signal transmission to the delay line.Transmission delay of the structure of the role, there are two: one is able to generate the clock cycle Ts 3.3 ns periodic oscillation signal, the second is surplus can be less than one clock cycle time interval to START and STOP ' 'displayed in the form of time value.Periodic oscillation signal cycle is determined by the delay ring, ring every run a circle is half of the clock cycle.

Only START signal to participate in the ring in this structure, each lap contains a nand gate and seven transmission delay unit.The beginning START signal is placed in a low level which is 0, ring is in a stable state, the R8 output of 1.On the first lap, the START signal rise along the spread into two input nand gate began to spread in the ring, rising into a falling edge.After the START signal into the ring in the logic 1 state, can make the signal transmission time and time again in the ring, until the STOP signal to arrive.In the second lap, the START signal at the R8 from 1 to 0, as feedback signal transmission to the nand gate, in the nand gate output signal from 0 to 1.Thus it can be seen in the R1, falling edge on the first lap signal form, into a rising along the second lap, so odd circle START signal transmission, in the form of falling edge even in the form of rising along the transmission.

When the STOP signal to L1, START signal can be either rising or falling edge in spreading, may be more than half of the clock cycle, in order to be able to effectively extract the sampling to the signal accurately, so added behind a two input nand gate and N is the same as the front structure of delay unit, which makes the START signal after the R8 can continue to spread.When the rest of the START and STOP time intervals of less than half a clock cycle, STOP to L1 START signal in the form of falling edge within the delay loop a delay unit, for example in R5, R5 and L1 signal again after R9 and L9 respectively into rising edge, deal with the two chains of the last rise along the signal can be the remaining time interval.When the rest of the START and STOP the rest of the time interval when more than half of the clock cycle, due to falling edge START signal at the STOP haven't arrived at L1, has been turned into a rising along the R1, but there is a path is a R9 into climbing along the transmission, when the STOP signal to L1, the START signal is a delay from the outer ring units, such as R13, need sampling is L1 and R13 signal, although the STOP signal is falling edge right now, but will become a rise after L9 along, still dealing with the two chains of the last rise along the signal can be the remaining time interval.From the above analysis it can be seen at the back of the delay line must be greater than delay loop delay time.

3.3 The coarse interpolation & synchronizer

Figure 7 is coarse interpolation apparatus & synchronizer structure, is consists of two parts, the coarse interpolation and synchronizer, there are both coarse interpolation counting function and the function of synchronous sampling.Coarse interpolation transmission START 'signal, is mainly composed of 12 transmission delay for 356 ps voltage-controlled delay units.Each delay unit in the state of STOP 'arrival can be D flip-flop, according to each output state D flip-flop situation determine START' position, then the encoder output NC.There are parasitic capacitance of the MOS tube, so STOP 'signal to connect the control end of the 12 D flip-flop will have an impact on signal rise time, this will lead to delay a D flip-flop output results.Assume that START after the seventh delay unit, 'STOP' arrival, DFF output should be 000000011111, but the actual output for 000000001111, when designing the encoder output for 1000, is the eighth still count as delay unit, the coarse interpolation count didn't make much difference.

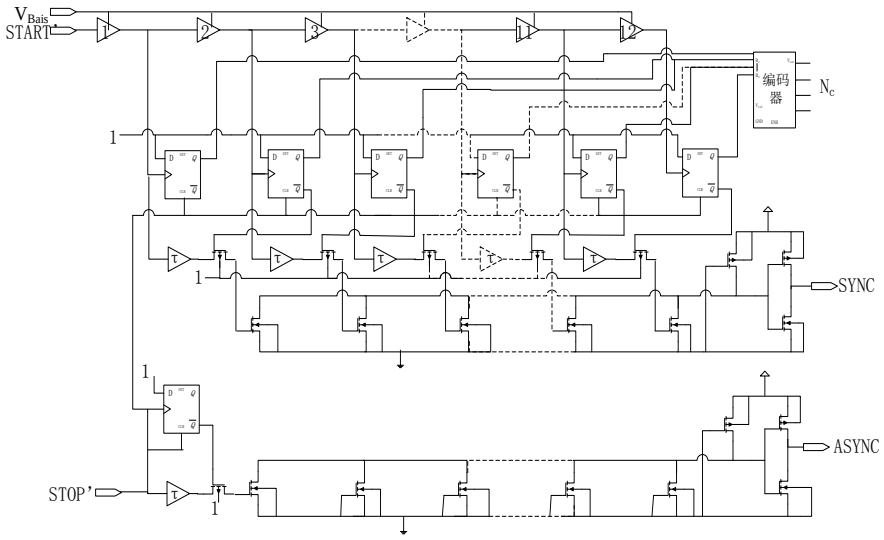

Fig.7 Coarse interpolation & synchronizer

Fine interpolation counter's mission is to measure the STOP signal and then START a delay unit under 'rising along the interval between the signal, the function of the synchronizer is to extract the two signals, such as extraction cases on the STOP signal' rise along with rising along the eighth delay unit.Every signal delay unit after the same delay tau can selectively by PMOS tube, the last two extracted by 11 NMOS input or goalkeeper.Get the stop 'arrival delay unit rise along is the key point of the circuit, because of the stop' did not arrive, D flip-flop is zero state, PNOS tube is a switch tube, controlled by the reverse D flip-flop output, is closed at this time.STOP 'arrival, D flip-flop from delay unit along the control output, due to the STOP in front of the' not the delay unit had arrived at, delay 0 remains the same, only the back of the delay unit have a rising edge, output 1 D flip-flop, reverse 0, PMOS tube open, make up along by, to extract the signal sampling.Due to the D flip-flop output will delay a D flip-flop, so use the next D flip-flop output to control a control unit output delays on the PMOS tube.Delay tau must be large enough, after the arrival of a PMOS transistor control to the control signal, delay unit rise along the signal to reach the PMOS tube, can appear otherwise error, uncertainty affect the extraction result.PNOS tube not only has simple structure, can reduce some mismatch error, but also because of PMOS tube can only transport rising edge, and the signal processing circuit also only to rise, so the use of a PMOS tube as switch control, it also can reduce the quantization error.

STOP "signal will pass through the same delay time to offset the START 'delay error signal, the route so he must be one of the unit delay the route signals are exactly the same.

3.4 Based on wiener ring fine interpolation

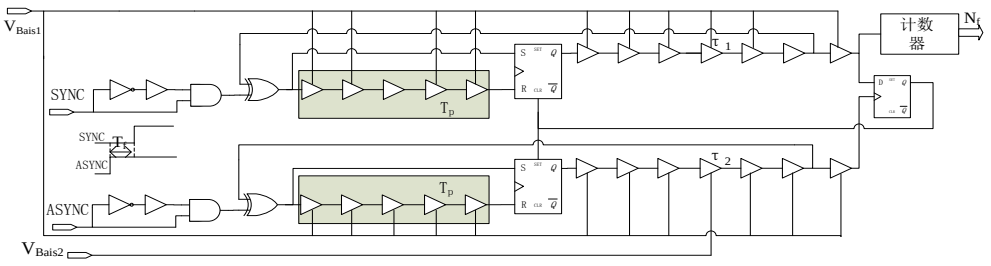

Fig.8 Fine interpolation counter

Figure 8 is based on the fine interpolator ChanJie wiener ring structure, each lap only a pair of wiener delay unit, which USES two chain delay unit and tau tau 1 2 propagation delay differential principle, make a resolution of 10 ps.This structure has two delay line and ASYNC signal transmit SYNC signals, respectively, in SYNC line unit propagation delay than the propagation delay of the unit in the ASYNC line is small, so the SYNC signals in the original behind the ASYNC, gradually will overtake

ASYNC signal.Compared with wiener ring structure with multiple delay element, not only reduced the number of delay unit, also reduce the number of the trigger, can reduce the occupied area, and even reduce the mismatch error of each delay unit, enhancing degree of linearity.Two delay unit and tau tau 1 2 bias by VBais1 and VBais2 control, other delay unit is controlled by VBais1 ring.In order to control the working state of the circuit, using the D flip-flop as a judge should cut, when the SYNC signals lag ASYNC, 0 D flip-flop, RS trigger input signal at the ends of the R and S, when the SYNC signals ASYNC in advance, 1 D flip-flop output, the output of the RS flip-flop results remain the same.Again in both the RS flip-flop can produce the same periodic signal pulse width, pulse width of the trigger the two input signals of R and S decision, namely Tp circuit to prevent distortion, loss of information.Overtake ASYNC SYNC signal, the measurement ends, running laps is NF measure results.

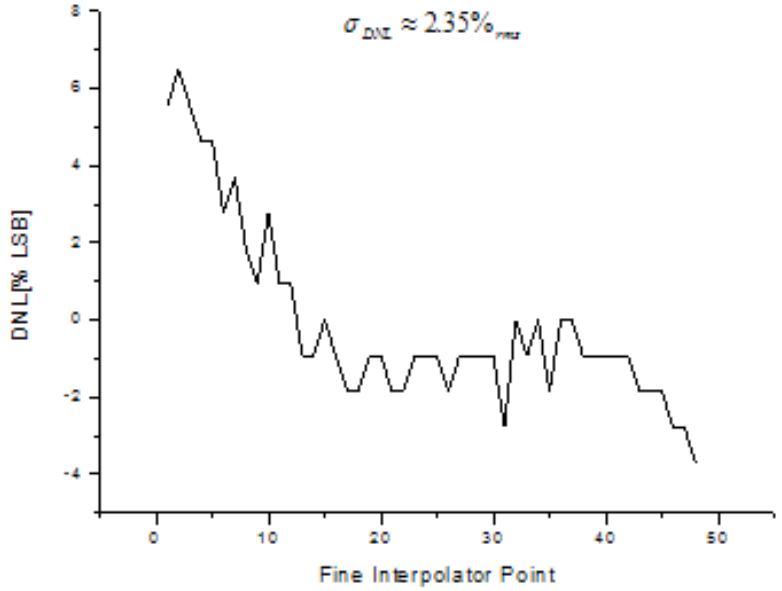

Fig.9 Fine interpolation counter DNL

Figure 9 is the essence of the interpolation of DNL counter each lap time delay simulation results, due to the fine interpolation counter counts most 36 circle, so just 1 to 36 times in DNL analysis, it can be seen that fine linearity interpolation counter is very good, its standard variance 2.35% RMS.

4. TDC simulation results analysis and discussion

In cadence 0.18 CMOS technology to realize the whole circuit, the working voltage of 1.8 V, the structure of time interval is obtained by the following formula:

$$T=3.3ns*N_s+356ps*N_c-10ps*N_f \quad (4)$$

The NS is a 6 bit counter measurements, a maximum of the whole circuit measurement is determined by the NS, NS maximum measuring 63 here.NC is coarse interpolation & synchronizer bit 4 measurements, representing the START signal 'position. Nf was pure interpolator 6 bit measurements. TDC circuit of variable ratio R = 10 ps, is also fine interpolator two chains in the VBais1 = 1.45 V, VBais2 = 990 mv, two delay time delay unit.

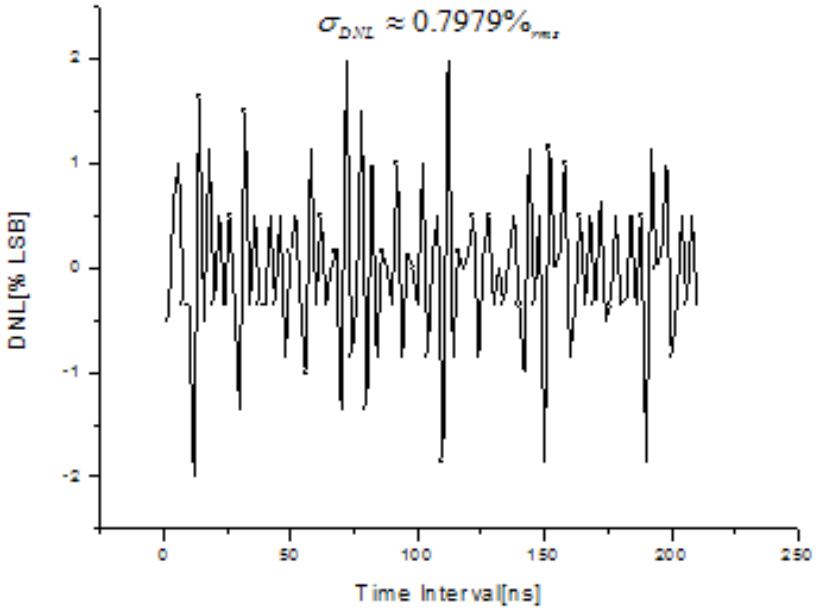

Fig.10 DNL

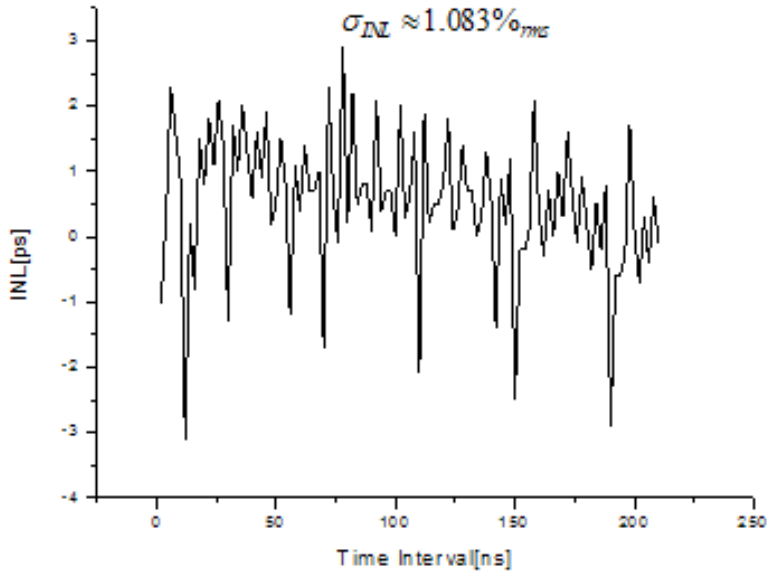

Fig.11 INL

TDC circuit using a ChanJie wiener ring structure of fine interpolation, got a very good DNL, can see from figure 10.In this structure the START and STOP signals without accumulation, so measuring the multiple sets of data, the RMS about 0.008 LSB, the DNL TDC DNL in the range of 0.02 LSB < DNL < 0.02 LSB.Figure 10 is the integral nonlinear TDC, INL range is 0.03 LSB < INL < 0.03 LSB, measuring the INL root mean square of about 0.011 LSB, effective (RMS) of 11 ps precision.

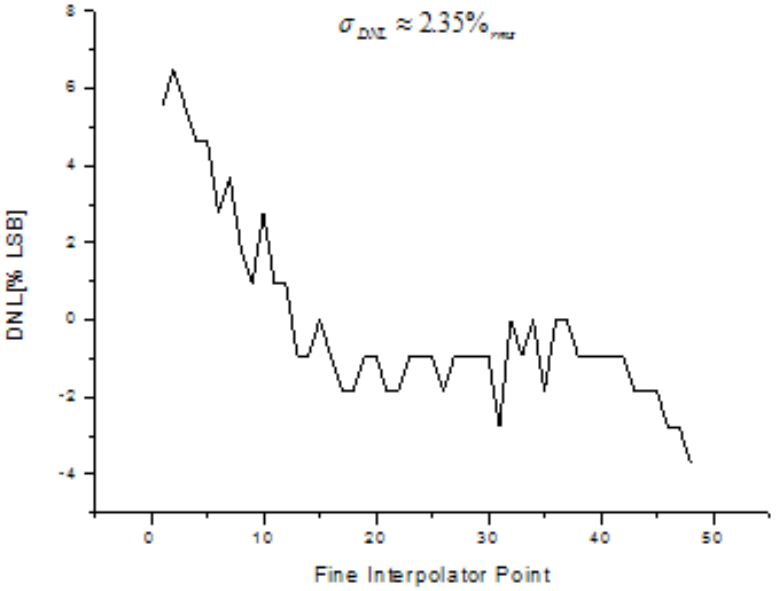

Fig.9 Fine interpolation counter DNL

5. Conclusion

This paper proposes a high linearity high resolution wiener ring time to digital converter.In 0.18 CMOS process, the working voltage of 0.18 V, by using the periodic oscillation signal propagation delay structure of 3.3 ns, the measurement dynamic range of 208 ns.Introducing wiener ring technology coarse - finishing two level interpolation, the resolution up to 10 ps.The introduction of wiener ring technology also enables the TDC circuit has good linearity, integral nonlinear precision less than 0.008 LSB, effective precision of the TDC circuit 11 ps.This structure is the combination of ring and two level interpolation, and reduce the use of a set of interpolator, performance is also improved.

Acknowledgements

Natural Science Foundation.

References

[1] Jansson J P, Koskinen V, Mantyniemi A, et al. A Multichannel High-Precision CMOS Time-to-Digital Converter for Laser-Scanner-Based Perception Systems[J]. IEEE Transactions on Instrumentation & Measurement, 2012, 61(9):2581-2590.

[2] Abas M A, Russell G, Kinniment D J. Embedded high- resolution delay measurement system using time amplification[J]. Iet Computers & Digital Techniques, 2007, 1(2):77-86.

[3] Yousif A S, Haslett J W. A Fine Resolution TDC Architecture for Next Generation PET Imaging[J]. Nuclear Science, IEEE Transactions on, 2007, 54(5):1574-1582.

[4] Villa F, Lussana R, Bronzi D, et al. CMOS Imager With 1024 SPADs and TDCs for Single-Photon Timing and 3-D Time-of-Flight[J]. IEEE Journal of Selected Topics in Quantum Electronics, 2014, 20(6):364-373.

[5] Torres J, Aguilar A, García-Olcina R, et al. Time-to-Digital Converter Based on FPGA With Multiple Channel Capability[J]. IEEE Transactions on Nuclear Science, 2014, 61(1):107-114.

[6] Cui K, Ren Z, Li X, et al. A High-Linearity, Ring-Oscillator-Based, Vernier Time-to-Digital Converter Utilizing Carry Chains in FPGAs[J]. IEEE Transactions on Nuclear Science, 2017, 64(1):697-704.

[7] Chen C C, Lin S H, Hwang C S. An Area-Efficient CMOS Time-to-Digital Converter Based on a Pulse-Shrinking Scheme[J]. Circuits & Systems II Express Briefs IEEE Transactions on, 2014, 61(3):163-167.
[8] Pekka Keränen, Kostamovaara J. A Wide Range, 4.2 ps(rms) Precision CMOS TDC With Cyclic Interpolators Based on Switched-Frequency Ring Oscillators[J]. Circuits & Systems I Regular Papers IEEE Transactions on, 2015, 62(12):2795-2805.
[9] Yu J, Dai F F, Jaeger R C. A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13 um CMOS Technology[J]. IEEE Journal of Solid-State Circuits, 2010, 45(4):830-842.
[10] Markovic B, Tisa S, Villa F A, et al. A High-Linearity, 17 ps Precision Time-to-Digital Converter Based on a Single-Stage Vernier Delay Loop Fine Interpolation[J]. Circuits & Systems I Regular Papers IEEE Transactions on, 2013, 60(3):557-569.Z.W. Zhang, J.N. Wang: Crane Design Manual (China Railway Press, China 1998), p.683-685. (In Chinese)