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Circuit Design of LWD 3D Holographic Azimuthal Electromagnetic Wave Resistivity Tool

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Abstract

The LWD 3D holographic azimuthal electromagnetic wave resistivity tool is a cutting-edge technology in the oil and gas exploration and development industry. Circuit design for such a tool faces challenges of harsh working environments with high temperatures, high vibration and shock level, limited board-mounting space, and complex functions. In response to these challenges, a scheme of low-power, low-noise, miniaturized and modular design is applied on the base of high-performance and high-temperature electronic components such as AD9832BRUZ and SM320F28335PTPS. In addition, real-time processing of large amounts of data is achieved by the combination of DSP with FPGA, and multiple communication methods are implemented for internal and external information exchanges. The DDS signal generation circuit creates 100kHz, 400kHz, and 2MHz sinusoidal RF signals with phase resolution of 0.09° and frequency resolution of 0.006Hz. The master DSP circuit implements multiple functions, such as signal generation, system communication, data processing, data storage, etc. The circuit system features with high stability, high data transmission rate, low power consumption and other advantages. In this paper, we focus on the system architecture, along with the detailed description of the designs of DDS signal generation circuit, the master DSP circuit and the communication circuit.

Keywords

3D Holographic Measurement; Electromagnetic Wave Resistivity Logging; Azimuthal LWD Logging; DSP; FPGA; DDS; Circuit Design.

1. Introduction

Electromagnetic wave resistivity logging while drilling has undergone significant advancements, from conventional resistivity measurements to 3D holographic azimuthal measurements. The tool not only detects adjacent formation interfaces but also determines formation anisotropy while measuring formation resistivity [1-3]. The detection range has improved significantly, from less than one meter to several meters, or even tens of meters [4-6]. Research and development efforts by international oilfield technology service companies such as Schlumberger, Halliburton, and Baker Hughes, among others, have been focused on the development of related technologies [7-10].

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Figure 1 shows the antenna configuration of our recently developed 3D holographic azimuthal electromagnetic wave resistivity logging (3DHAEM) tool, which comprises four axial transmitter antennas, two transverse transmitter antennas, two axial receiver antennas, and four oblique receiver antennas. The instrument acquires the phase and amplitude of electromagnetic wave signals at different frequencies with different transmitter-receiver pairs to obtain our target measurements, such as formation resistivity, formation interface position and orientation, and formation anisotropy. To achieve azimuthal measurement, the acquired signal is recorded by sectors as the instrument rotates, with a circle round being typically divided into 16 (8 or 32) sectors. The instrument uses FPGA and DSP as the core for data processing and achieves signal fidelity, along with high-speed ADCs. Figure 2 shows the FPGA signal acquisition and processing procedures. The amplitude and phase of the signal are obtained by DFT computation of the sampled data in the FPGA. Further data calculations are performed on the master DSP producing conventional formation resistivity, azimuthal resistivity, anisotropy signal, and adjacent interface position/distance.

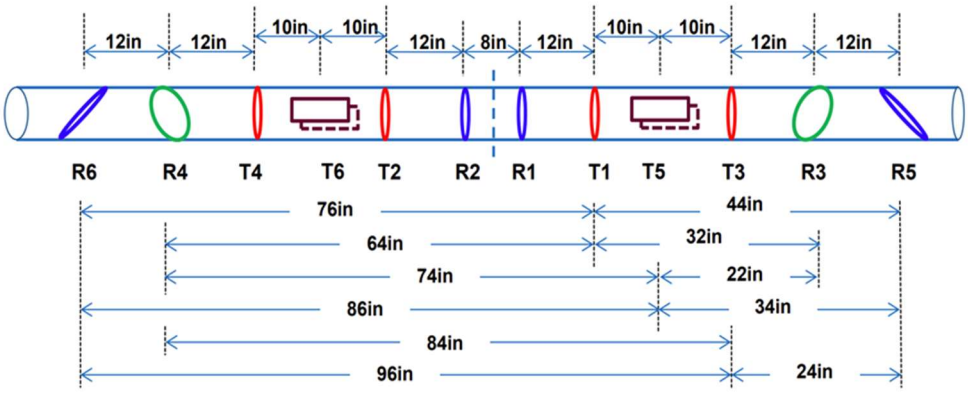

Figure 1. Antenna configuration of the 3DHAEM tool

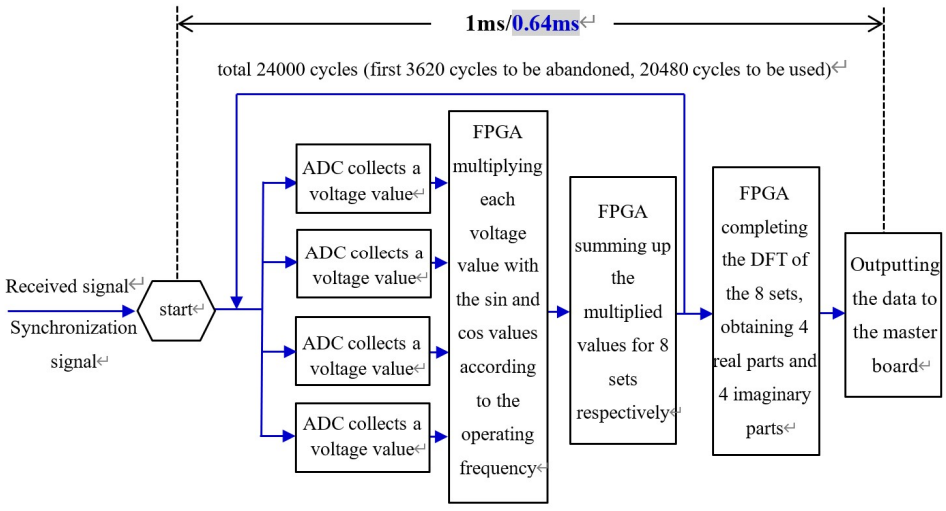

Figure 2. FPGA signal acquisition and processing

Because the 3DHAEM tool acquires azimuthal measurements for six transmitters and three operating frequencies, the design of the circuit system becomes exceptionally complex, making it a key aspect of the entire instrument development. The master control circuit forms the core of the system, with the transmitter circuit and receiver circuit being the vital elements. Technical key points include DDS-based signal generation circuit design, DSP-based synchronization and data processing circuit design,

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and DSP-based communication circuit design. This paper focuses on the system design and key circuit design of the 3DHAEM tool, along with the description of related function requirements and working principles.

2. System Architecture

As the 3DHAEM tool operates in downhole environments, the circuit system must withstand high temperature, high pressure, and strong vibrations and shock [11]. In addition to achieving multi-functions, including signal generation, signal reception, data processing, and system control, all electronic components and circuit boards need to be designed to be temperature-resistant, pressure-resistant, and vibration-resistant. Circuit boards are designed to be as small as possible while preserving their full functionality due to the limited board-mounting space. To cater to different work scenarios, a modular scheme is applied to divide the circuit system into ten boards, making the circuit system easier to design, test, and maintain. Differential line pairs are used to facilitate communication between boards, significantly reducing mutual interference during signal transmission and enhancing the signal-to-noise ratio and measurement stability.

Figure 3 shows the overall circuit scheme for the 3DHAEM tool. The system comprises ten components: the master board, the transmitter board, the matching board, the preamplifier board, the receiver board, the power filter board, the power supply board, the universal modem board, the magnetic sensor board, and the azimuth measurement board. The master board generates sinusoidal RF signals at different frequencies and transmits them out-wards through the differential signal lines. The transmitter board amplifies the signal from the master board. The sinusoidal RF signal then passes through the matching board, which ensures the maximum current flowing through the transmitter antenna, transmitting the electromagnetic wave to the formation and borehole. A voltage signal is detected at each receiver antenna when the electromagnetic signal propagates through the strata. The receiver signal is amplified and filtered through the preamplifier board and the receiver board before the A/D conversion. The ADC outputs are processed in the FPGA to conduct the DFT transformation. These data are transmitted to the master board for further computation.

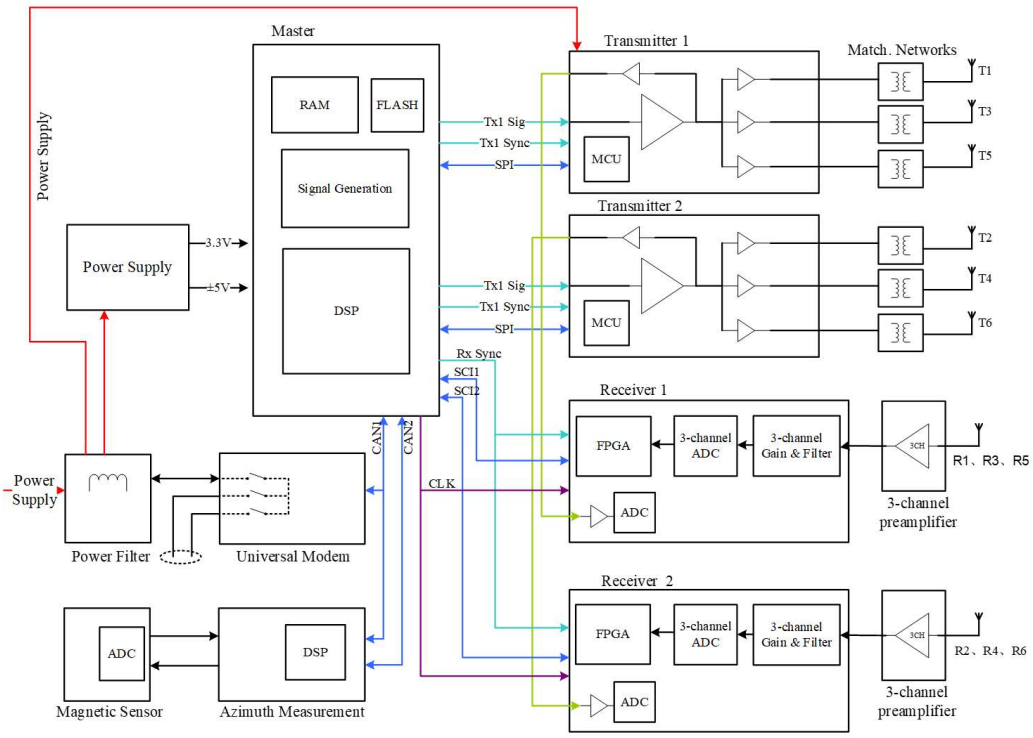

Figure 3. System architecture of the 3DHAEM tool

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The vital circuits in the system of the 3DHAEM tool include the DDS signal generation circuit, the master DSP circuit, and the communication circuit. The DDS signal generation circuit is responsible for generating a high-resolution sinusoid RF signal with adjustable amplitude, which plays a key role for the precision of the measurement. Higher precision sinusoid RF signals make the measurement more precise. The master DSP circuit is responsible for controlling the entire system and processing of the received signal. The communication circuit mainly implements functions such as data flow between the tool and the surface computer, data monitoring of the circuit system, and data exchange between different boards. A detailed description of the DDS signal generation circuit, the master DSP circuit, and the communication circuit will be given as follows.

3. Critical Circuit Design

3.1 DDS Signal Generation Circuit

Various methods can be used to generate sinusoid RF signals, including direct analog frequency synthesis based on crystal oscillators, phase-locked loop digital frequency synthesis (PLL), and direct digital synthesis (DDS) [12-14]. This system requires output sinusoidal RF signals at operating frequencies of 100kHz, 400kHz, and 2MHz. The signal must have high precision in amplitude and phase, and the operating frequency needs to be switchable at any time. We, therefore, opted for the signal generation scheme based on DSP and DDS.

Figure 4 shows the structure of DDS, consisting of a phase accumulator, a sine lookup table, a D/A converter, and a low-pass filter [15, 16]. The phase accumulator performs phase accumulation of the frequency control word under the action of the clock signal. The phase-to-amplitude conversion at the sine lookup table is accomplished under the phase accumulator's signal output. The sinusoidal RF signal at a particular frequency goes through the D/A converter and the low-pass filter before outputting.

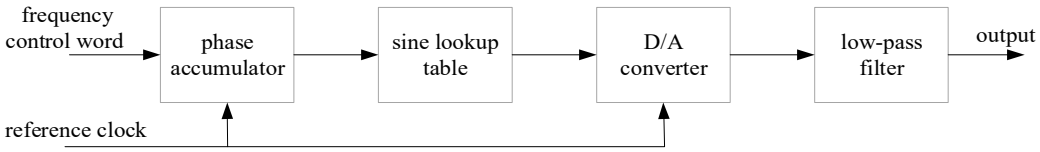

Figure 4. Basic Structure of DDS

We chose AD9832BRUZ as the DDS chip for the 3DHAEM tool. This chip features with a 32-bit phase accumulator, a sine lookup table, and a 10-bit DAC. It supports register loading via serial interfaces and can achieve phase and frequency modulation at clock rates of up to 25 MHz. A high-temperature crystal oscillator in the peripheral circuit provides actively a 24MHz clock signal to the DDS. The frequency and phase of the output signal of AD9832BRUZ are calculated using the following formula:

$$f = \Delta Phase \times f_{MCLK}/2^{32} = f_{MCLK}/2^{32} \times FREQREG$$
$$Phase = 2\pi \,/\, 2^{12} \times PHASEREG \quad (1)$$

Shown in Figure 5 is the DDS signal generation circuit. The REFin pin serves as the reference voltage input pin, providing a 1.21 V input reference voltage through voltage divider resistors. The MCLK pin serves as the input clock pin with a frequency of 24MHz. The FSEL pin is used to select the frequency register, and the phase register is controlled by the PSEL0 and PSEL1 bits. The FSYNC pin, SDATA pin, and SCLK pin are logic input pins. The configuration for the DDS is being loaded from the DSP via McBSPa interface. At a reference clock of 24MHz, the program outputs 2MHz,

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400kHz, 100kHz, and 0-phase sine wave command controls to be written in the order shown in Table 1.

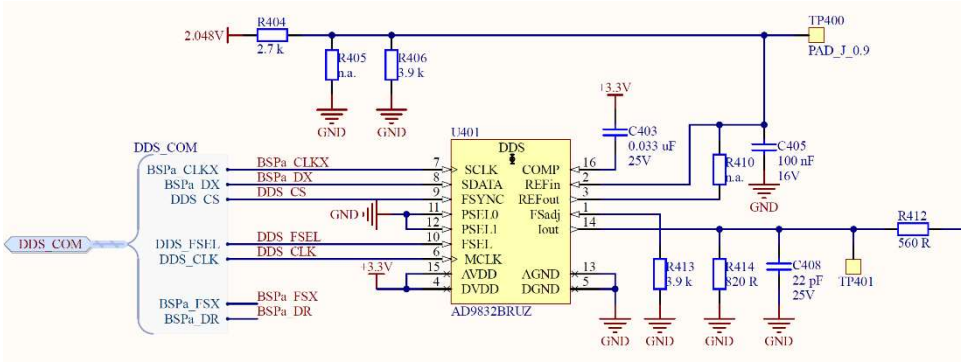

Figure 5. DDS signal generation circuit

Before entering the transmitter board, the sinusoidal RF signal generated by the DDS must be amplitude modulated. In Table 2, five different output levels of the sinusoidal RF signal are defined according to the needs of the transmitter board. The levels can be switched upon the input control signal of the signal amplitude modulation circuit, as shown in Table 3. To achieve different output levels, an operational amplifier combined with an analog switch is used, and the circuit is schematically shown in Figure 6. The analog switch regulates the amplitude of the sinusoidal RF signal based on the control signal. The performance of the operational amplifier is crucial to the accuracy and speed of the generation of the sinusoidal RF signal. The LT1355 operational amplifier is chosen for its high bandwidth, low noise, and low power consumption, while, the HI-8190PSTF analog switch is selected for its low R_ds_on and low parasitic capacitance.

Table 1. DDS control commands

Command and Control	2MHz	400kHz	100kHz
Reset	0xD000	0xD000	0xD000
Frequency Register 0 LLSB	0x3055	0x3044	0x3011
Frequency Register 0 HLSB	0x2155	0x2144	0x2111
Frequency Register 0 LMSB	0x3255	0x3244	0x3211
Frequency Register 0 HMSB	0x3415	0x3404	0x3401
Phase Register 0 LSB	0x1800	0x1800	0x1800
Phase Register 0 MSB	0x0904	0x0904	0x0904
Set SELSRC	0x9000	0x9000	0x9000
Exit Reset	0xC000	0xC000	0xC000

Table 2. DDS output levels

Name	Minimal	Low	Medium	High	Maximal
Voltage(pk-pk)	265mV	390mV	480mV	745mV	1.05V

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Table 3. Control signals of analog switch

Gain level	DDS_Gain_1x	DDS_Gain_2x	DDS_Gain_p5	DDS_Gain_p0625
Minimum	1	0	1	1
Low	1	0	0	1
Medium	0	1	1	1
High	0	1	0	1
Maximum	0	1	1	0

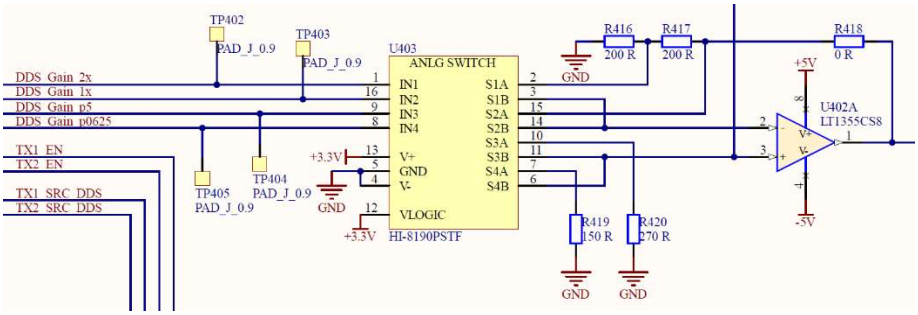

Figure 6. Analog switch-controlled amplifier circuit

To enhance the driving capacity of the sinusoidal RF signal, additional operational amplifiers need to be added as driving circuits. A fully differential in-phase amplifier driver circuit is designed with a gain of one as shown in Figure 7. The output is a differential signal, which improves the anti-jamming capability of the signal while ensuring the reliability of the data transmission. The formula of the calculation of the output gain of the drive circuit is A_V=R_422/R_421 . Changes can, therefore, be made by adjusting the values of R421 and R422. The core device of this circuit, THS4521HD, is a low-power, fully differential operational amplifier that operates at extreme temperatures ranging from -55 ℃ to 210 ℃. The THS4521 features with accurate output common-mode control that allows for dc-coupling when driving ADCs.

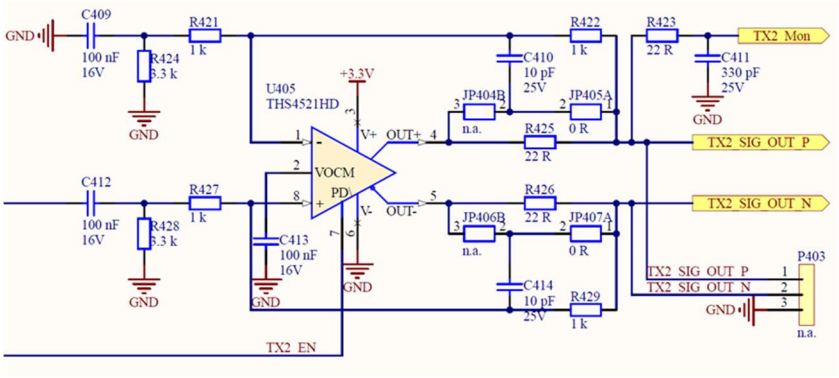

Figure 7. Fully differential in-phase amplifier driving circuit

3.2 Master DSP circuit

The DSP on the master board acts as the control and processing core of the entire circuit system. It processes the collected receiver signal to produce amplitude and phase data, which are then stored in the memory module. Additionally, the circuit generates control signals sent to the MCU and FPGA through different buses to execute various functions including starting/stopping the instrument, switching between operating modes, controlling the amplitude of transmitted signals, timing and synchronization.

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The DSP used is SM320F28335PTPS, featuring with low power consumption and high performance. It is capable of operating for extended long periods of time in high temperature environments. Figure 8 shows the DSP, along with its peripheral circuits. The device's primary features and functions are as follows: (1) The high-performance 32-bit CPU operates at a 150MHz main frequency with a 6.67 ns core instruction cycle when the core voltage is 1.9V. It is capable of processing complex mathematical algorithms through C/C++ and assembly language programming and offers quick interrupt response and data processing. (2) The device has a 12-bit A/D converter, is equipped with a 2×8 channel input multiplexer, constituting 16 analog input channels, gathers power supply voltage in the master board and current of the transmitter board. The data conversion cycle is 80ns. (3) The device features with three groups of SCI interfaces that can support standard asynchronous communication mode: the SCIa communicating with the upper receiver board, the SCIc communicating with the lower receiver board. (4) There are two configurable McBSP interfaces, one is connected to the DDS to control the generation of the sinusoidal RF signal, and the other is connected to two transmitter boards to regulate signal transmission timing. (5) It has two CAN interfaces, one SPI interface, one I2C interface. It also has 88 GPIO interfaces that can be configured via software as special functions or universal I/O interfaces. The CAN interface, which has a communication rate of up to 1Mbps, is connected to a universal modem board and an azimuth measurement board for control and communication purposes. The SPI interface, which can program the communication rate and the length of the communicated data, is connected to flash on the master board to quickly read the parameters and data stored therein. (6) Having a JTAG interface for program download, online simulation, and program debugging. (7) The external crystal oscillator is connected to the DSP via the XCLKIN pin to provide actively a clock signal to the system.

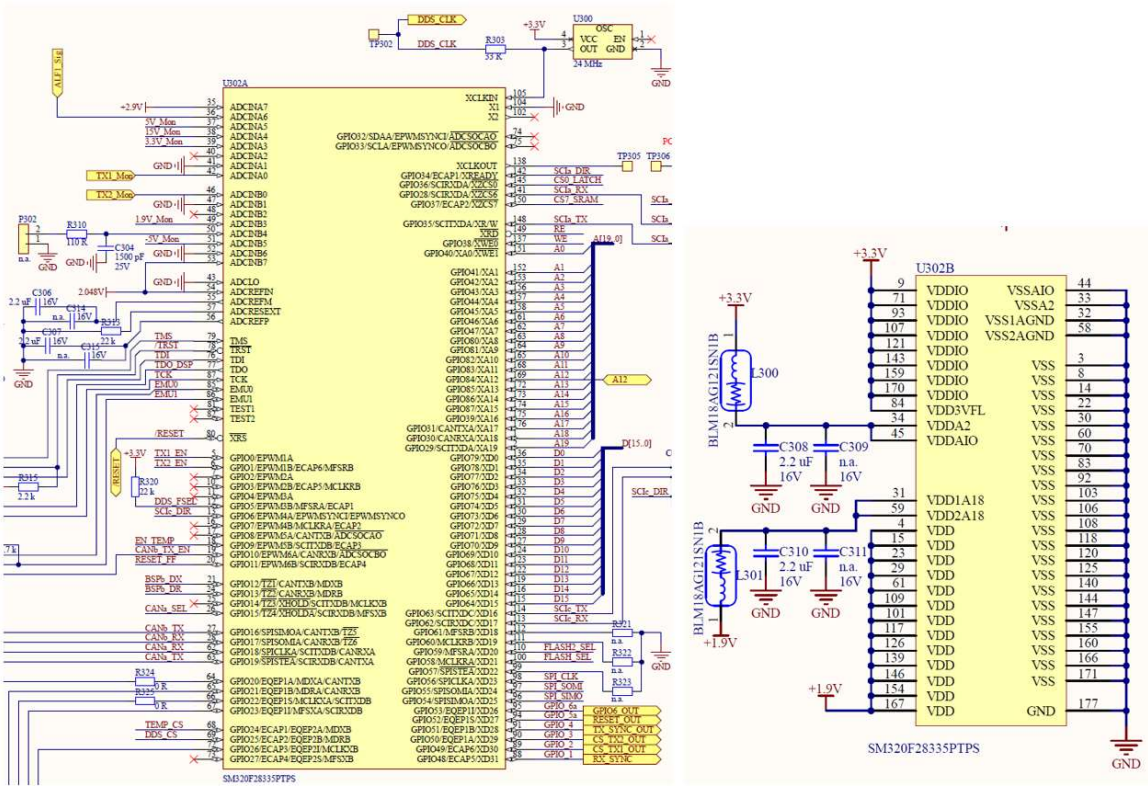

Figure 8. Master DSP and peripheral circuit

3.3 Communication circuit

The circuit system achieves functions such as the data communication between the instrument and the upper computer, the status monitoring of the circuit system, and the data exchange between different boards via CAN, SCI, and SPI interfaces. The master DSP is a large-scale integrated circuit and lacks of power driving capability. Due to the large load that needs to be driven on the bus of the

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master DSP, a line driver is required to provide a power driver for the signal. Furthermore, the bus uses a time-sharing multiplexing method for the signal transmission, whereby the signal at the pin changes during different time periods. To separate and store the signals, a line driver acting as a latch is necessary.

The high-speed differential CAN interface transceiver used is SN65HVD233HD. Figure 9 shows the schematic of the designed CAN transceiver circuit. The transceiver is stable in harsh environments of high temperatures, high voltages and strong vibrations, and has a signal transportation rate of up to 1 Mbps. The transceiver features with cross wire, overvoltage, and loss-of-ground protection to ±36 V, with common-mode transient protection of ±100 V.

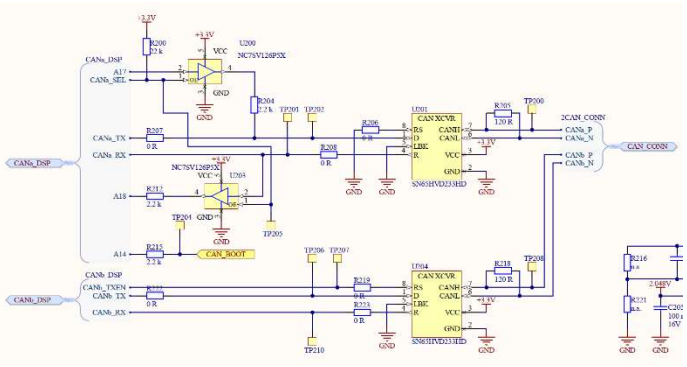

Figure 9. CAN transceiver circuit

The master board communicates with and controls the transmitter board to enable/disabled the channel and read out temperature sensor of the transmitter board via SPI. Figure 10 shows the schematic of the SPI driving circuit. The SPI interface is connected from the DSP McBSPb interface to the upper and down transmitter boards. Two chip selection lines (CS_TX1/ CS_TX2) distinguish between the different transmitters. The SPI line driver employed in the circuit is SN65LVDM176DGK, which can support signal transportation rates of up to 400 Mbit/s and operate for significant periods under high temperature conditions. The bus pins have ESD protection of more than 15 kV. When disabled or when the VCC drops below 1.5 V, the bus pin has an elevated impedance.

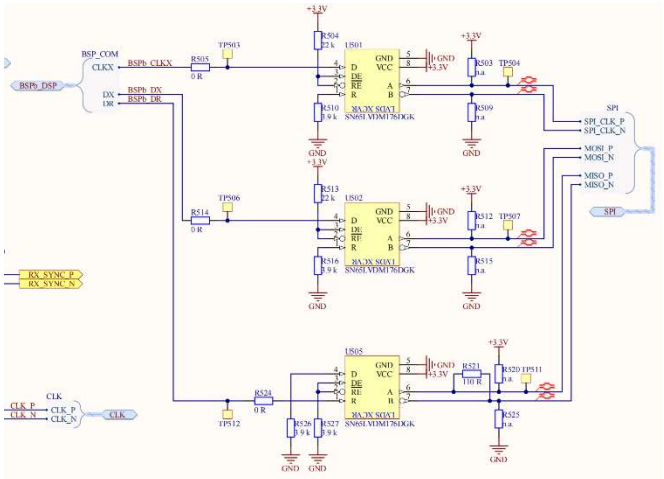

Figure 10. SPI driver circuit

SN65LVDM176DGK is used as the SCI line driver, shown in Figure 11. The master DSP communicates with the two receiver boards through two distinct SCI interfaces: SCIa for the upper

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receiver board and SCIc for the lower receiver board. These buses facilitate the control of receiver activities, including data sampling and data processing.

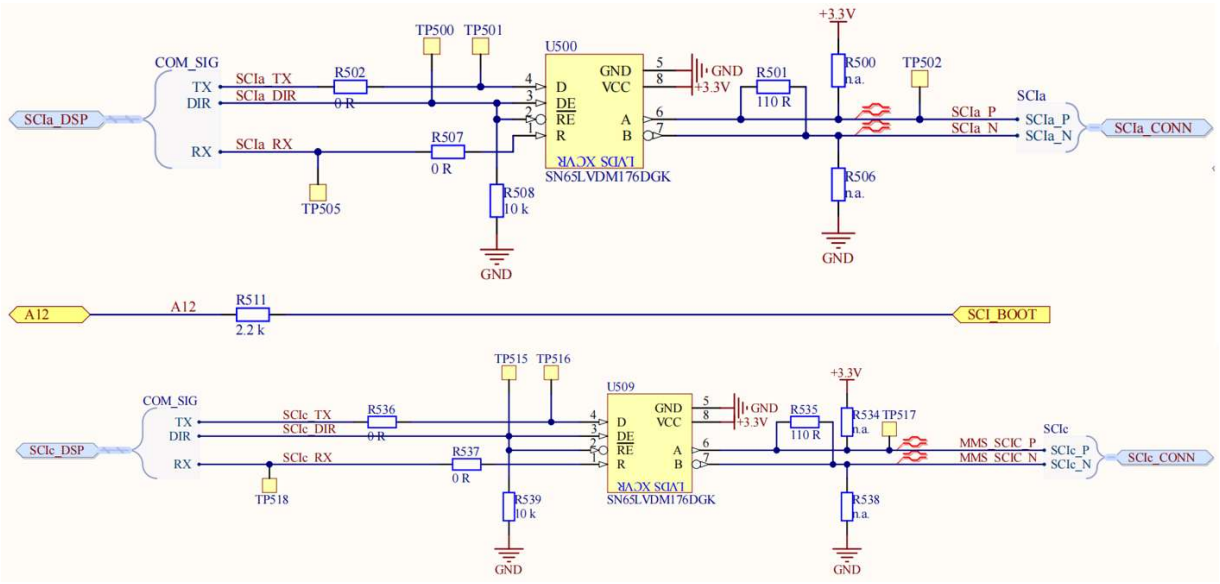

Figure 11. SCI driver circuit

4. Software Process

Based on hardware design, 2MHz, 400kHz, and 100kHz signals are transmitted for 1ms respectively. The signal of each frequency undergoes switching after 1ms, and this process continues. The design process is shown in Figure 12.

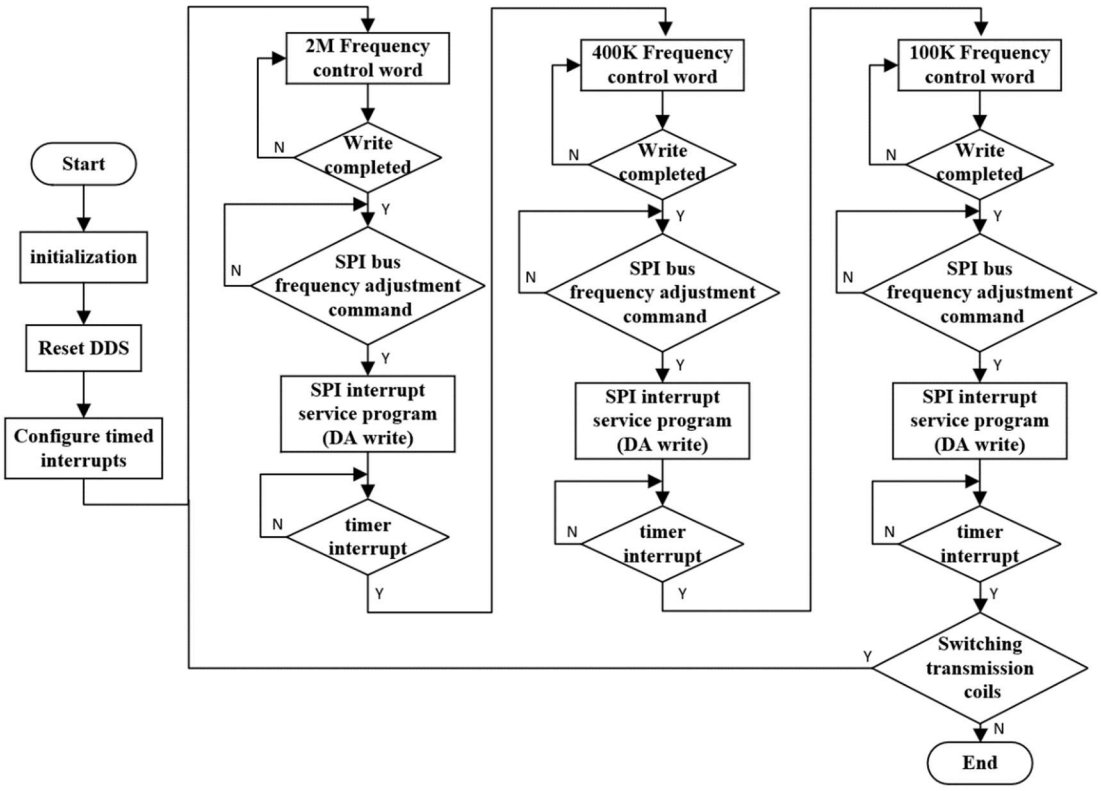

Figure 12. Program flow

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5. Test Verification

The DDS chip generates 2MHz, 400kHz, and 100kHz transmit signals, which are filtered through the network and shown in Figure 13. The frequencies measured by the oscilloscope are 2.00004MHz, 400.007kHz, and 100.001kHz, respectively. The signal frequency accuracy is very high, which can meet the frequency requirements of the instrument's transmit signals.

(a) 2MHz (b) 400kHz (c) 100kHz

Figure 13. Transmit signals

6. Conclusion

The 3DHAEM tool is a cutting-edge technology in the oil and gas exploration and developement industry. Circuit design for such a tool faces challenges of harsh downhole working environments with high temperatures and high vibration level, limited board-mounting space, and complex functions. In response to these challenges, a scheme of low-power, low-noise, miniaturized and modular design is implemented on the base of high-performance and high-temperature electronic components. In addition, real-time processing of large amount of data is achieved by the combination of DSP with FPGA, and multiple communication methods are applied for internal and external information exchanges.

The key circuits of the tool include the DDS signal generation circuit, the master DSP circuit, and the communication circuit. The DDS signal generation circuit generates 100kHz, 400kHz, and 2MHz sinusoidal RF signals with phase resolution of 0.09 ° and frequency resolution of 0.006Hz. The master DSP circuit implements multiple functions, such as signal generation, system communication, data processing, data storage, etc. The circuit system features with high stability, high data transmission rate, low power consumption and other advantages.

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