Design of High Speed Communication System Based on FPGA

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Abstract
The content of the design is the serial communication between FPGA and FPGA, FPGA and PC, FPGAs are connectedly by RS-485, while the level translation between FPGA and PC is realized by MAX232 chip. Visual Basic is uses as programming language of master computer and VHDL is used as FPGA programming language.

Keywords
FPGA, MAX232, RS-485, VHDL

1. The Schemes of the Whole System
This design is mainly to realize the serial communication between FPGA and PC, FPGA and FPGA , FPGA and MCU. So the whole system is mainly composed of three identical modules, as shown in figure 1

![Diagram of the whole system](Fig.1 Integrated module design)

2. FPGA Module Design
2.1 SCI Serial Interface Chip Design Introduce
This design is mainly using SCI chip to realize duplex communication between the serial port design. The SCI pin as shown in Figure 2, it has 20 pins, 17 of which are input and output pins effectively. SCI external pin:
(1) CLK - clock signal; (2) RESET - reset input; (3) RXD - serial data input;(4) RD - read signal input;(5) WR - write signal input;(6) CS - chip select input; (7) TXD - serial data output; (8) rdFULL - receive register "full" signal output;(9) tdEMPTY - send register "empty" signal output;
(10) D0~D7 - data bus input and output; in which, D0~D7 is a two-way three state input and output.
2.2 Serial Data Transfer Format and Synchronization Control Mechanism

(1) Serial data transfer format
SCI chip transmit serial data transmission by data format fixed. A data or a character is 10bit, including 1 start bit, 8 data bits or a character plus 1 parity, one stop bit. In order to position the correct operation, select each data bit should contain 4 clock cycles (CLK). In order to get the baud rate of serial data transmission, such as 9600bps, then the external clock should be selected for 38.4kHz.

(2) Control Mechanism For Serial Data Transmission
Asynchronous serial data transfer, because there is no dedicated to provide synchronization signals, it can only be extracted from the transmitted signal synchronization information, such as the starting position of the data for the SCI string and transform to provide a start signal.

2.3 Simulation Analysis
VHDL language used to describe the SCI chip, its procedures see appendix, simulation waveform as shown in Figure 3.

Fig.3 Sending and Receiving Process Simulation
This simulation diagram is the process of sending and receiving simulation. After SCI reset, send data control counter SCIT and receive data control counter SCI have been cleared, tdEMPTY for the "1", rdFULL for "0". SCI chip into the initial state. In order to receive process simulation, in the RDX signal line is a 1010101 string data that a 8-bit 55h value data. When rd= '0' and cs= '0' when, said the computer receives data, this is the s RdFULL_s becomes "0", indicates that the data has been read, computer will be the data bus of a data write send register DIN latch, and to sign rxdF operation, when the rxd= '0', that start to come. RxdF set "1": when there is a low level data on the receiving end RXD and a data arrival starts, receiving control counter SCI are arranged into 1010101 and the CS and WR appeared a for "0" negative to choose and write pulse. After the stop bit of the serial data, a negative gating pulse and read signal is arranged on the CS and the RD, and then the emulator is started. Then on
the TXD you can see a bunch of "01010101" of the transmission pulse, the data line in the data and read
the pulse corresponding position to get the 55H of the received data value. Simulation results show that
the working process is correct.

3. Serial Communication Between FPGA and PC

In this design, it is necessary to realize the serial communication between PC and FPGA, and PC only
two RS-232 serial interface to realize serial communication between them, requires a reliable
performance of RS-485 and RS-232 interface conversion. The design scheme of simple and reliable
conversion interface circuit without RS standard level and TTL level conversion chip is given.

4. Serial Communication Between FPGA and FPGA

The communication module between FPGA and FPGA is shown in Fig5.

Universal asynchronous serial receiver error checking mechanism is perfect, including start, stop
judging, data bits 0 and 1 of the judgment, the judgment error handling etc.. After experimental
verification, the communication rate is 1M bit/s, without changing the logic timing, communication
conditions can meet the 128kbit/s or 64kbit/s (rate of A or u rate) to multiplex voice communication.
The internal structure as shown in figure5. The bus data transceiver module is the key to realize high
speed communication. Used to complete and / serial conversion, asynchronous serial transceiver logic,
improve the data transceiver rate function clock module is used to complete the clock frequency,
resulting in a variety of CPU module and bus module requires a variety of clock frequency. The bus data
transceiver module can send and receive data at the rate of bit/s 1M. .

5. Serial communication between single chip microcomputer and FPGA

The serial communication module of single chip microcomputer and figure 6 is shown
AT89S51 which is produced by ATMEL company used. It is a high performance 8-bit COMS microcontroller. It is compatible with the MCS51 command system and 8052 pins. It is powerful and can be used in all kinds of complex control applications. AT89C51 has 8K erase duplication flash flash and ideal state can be erased 1000 times; 256X8 ram; three 16 bit timer/counter T0, T1, T2; 8 interrupt sources include timer/Counter interrupt, external interrupt, and the serial port interrupt; 32 can be programmed I/O port, which P0 port number according to low address multiplexing, P1.0 and P1.1 for timer/counter 2 port interrupt, P2 is the high-order address port, P3 is a general purpose I/O port and control port multiplexing port; the clock range for 0–24MHZ. The power down mode saves the contents of the RAM, and when the oscillator stops, the other parts are forbidden to work until the next hardware reset.

6. Conclusion

This topic in practice has a strong value, along with the rapid development of information, high in urgent need of a transmission rate of interface to realize serial communication, and the characteristics of FPGA is high transmission rate, integration, has broad application prospects. Therefore, it is necessary to research learning. Through the efforts to better accomplish the task of this task. To successfully realize the serial communication between PC and single chip microcomputer, must pay attention to four points: one is the communication format; second is the baud rate, both of which set must be consistent; the third is the response signal transfer between MCU and FPGA, if transmitting or receiving data error, by the receiver a signal transmitter requests resend; fourth, the serial communication between FPGA and pay attention to the timing design.

Reference