Design of Equal Precision Frequency Measuring Instrument Based on CPLD

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Abstract
This paper introduced a plan that using frequency precision measuring instrument designed to achieve the program. It is mainly based on the CPLD, the monolithic integrated circuit for auxiliary, with high-speed chip to pose a major CPLD logic count module. So as to design a frequency measuring instrument of measuring frequency range of 0 ~ 100 MHz, and in the whole frequency range can be achieved equal precision, frequency measurement accuracy can be achieved 1/1000000.

Keywords
Cymometer; Frequency Measurement; Equal Accuracy; CPLD

1. Introduction
In the modern electronic systems, the proportion of digital systems is growing. The digitalization and integration is the trend of system development, CPLD as programmable ASIC (application-specific integrated circuit) devices, it will plays more and more important role in digital logic system. And digital frequency meter is computers, communications equipment, audio, video, and other areas of the scientific research production indispensable measuring instrument.

In fast measurement requirements, to ensure high accuracy of frequency measurement must be used higher standard frequency signal; the microcontroller clock frequency unable to meet the high-speed, high-precision frequency measurement requirements by itself and several command calculating limits, and the measured frequency is slow. Using of highly integrated, high-speed CPLD provide a guarantee to achieve high-speed, high-precision frequency measurement. The frequency measurement system is divided into several functional modules, such as signal synchronization input, the control section, division and counting means, timing, and standard frequency signal amplification shaping module. The module can be integrated with other CPLD chip, and each logic module graphics hardware description language to describe its function, except for divisor, shaping and amplifying standard signal input, but by EDA development platforms, such as design documents MAXPLUS II done automatically compile logic, simplification of logic, integrated and optimized placement and routing logic, logic approach. Finally, CPLD Chip is programmed.

2. Select the measurement principle and the shutter time
And other precision frequency measurement method is: using accurate high frequency signal with a frequency as a standard frequency signal, to ensure measurement gate time is an integer multiple of the signal, while the standard pulse signal and the signal pulses are counted in the gate time, to achieve frequency accuracy over the entire frequency range equal, when the high frequency standard signal, and gate time is long enough, you can achieve high-precision frequency measurements.
And equal precision frequency measurement principle shown in Figure 1.

![Figure 1 Schematic and other precision frequency measurement](image)

The accuracy of measurement and the gate time relationship analysis is as follows.

Giving a high level by gate control signal (C), at this time, did not begin to wake frequency count, the beginning of the standard clock signal to wait until the arrival of the rising edge of the measured signal. When the gate control signal through the end of time, but also to wait until the arrival of the rising edge of the signal and stop signal and the signal standard count, read the count value at this time, the measured signal frequency measurement count simultaneously. Frequency measurement count gate time $dT$, standard clock signal frequency $sf$ , frequency of the signal to $xf$, pulse count value of the standard clock signal and the measured signal within the $dT$ time were $SN$ and $XN$, the frequency of the signal by the following formula:

$$xf = f_s \times \frac{N_x}{N_s}$$  \hspace{1cm} (2-1)

Timing error signal generated by the standard:

$$\Delta t = T_d - N_s \times X \times T_s$$  \hspace{1cm} (2-2)

Due to the maximum $\Delta t$ is a standard signal cycle, $\Delta t \leq T_s$, so:

$$xf = N_x / (N_s \times T_s) = N_x / (T_d - \Delta t)$$  \hspace{1cm} (2-3)

The exact value of the measured signal frequency $f_o = N_x / T_d$, the relative error of measurement of frequency:

$$\delta = \left( \frac{f_x - f_x O}{f_x O} \right) = \Delta t / (T_d - \Delta t)$$  \hspace{1cm} (2-4)

When $T_d$ is greater than $\Delta t$, the maximum error of frequency measurement:

$$\delta m = T_s (T_d - T_s) \approx T_s / T_d$$  \hspace{1cm} (2-5)

The final expression shows that when the biggest error of frequency measurement by the cycle of the clock signal $S$ gate time decision and frequency count $\delta m$, $S$ is smaller, $T_d$ is the bigger, measurement error is smaller, he accuracy of measurement is the higher. In the whole frequency measurement range, precision constant, implements the equal precision measurement. When selecting an accurate 40MHz standard signal signal source, $TS = 25ns$, in order to make the measurement of the maximum error $\leq 10^{-6}$, and accuracy is reached millionth.

$$T_d \approx T_s / \delta_m = 25ms$$  \hspace{1cm} (2-6)

Select gate time $T_d$ measurement, in addition to the maximum measurement error satisfies the formula $\delta m$, it should also be measured to ensure that more than one signal period $T_x$. The relative error of the measuring frequency has nothing to do with the size of the measured signal frequency, only related with the gate time and frequency standard signal, which realized the entire test frequency and other precision measuring. The longer the gate time, the higher the standard frequency, the frequency measurement relative error is smaller. Standard frequency can be stability, high precision frequency crystal oscillator, to ensure accuracy in the same premise, raise the standard signal...
frequency, can shorten the gate time, namely to improve test speed. Table 1 lists the standard screen at 40MHz, the gate time corresponds with the maximum permissible error.

<table>
<thead>
<tr>
<th>Gate time (S)</th>
<th>accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0025</td>
<td>$10^{-5}$</td>
</tr>
<tr>
<td>0.025</td>
<td>$10^{-6}$</td>
</tr>
<tr>
<td>0.25</td>
<td>$10^{-7}$</td>
</tr>
<tr>
<td>2.5</td>
<td>$10^{-8}$</td>
</tr>
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</table>

3. **Hardware circuit module**

Composition principle of the system block diagram shown in Figure 2. A CPLD to complete the testing capabilities of the standard frequency and the measured signals are counted. SCM control of the entire test system, including a keyboard and read signal processing; to CPLD measurement process control, measurement processing result data; final measurement results sent to the LED display output. The signal shaping circuit mainly for clipping the signal, amplified, and then the Schmitt trigger after shaping into the CPLD. With active crystal 50MHz as the test standard frequency of CPLD. 220V AC power supply part by the transformer, filtering, voltage regulator to give SV for the entire system. The device provides a standard by an external 12MHz crystal clock circuits.

![Figure 2 composition block diagram of the frequency meter based on CPLD](image)

CPLD and SCM are connected as shown in Figure 3.

![Figure 3 CPLD and SCM wiring diagram](image)

CPLD (EPM7128SLC-6) after plastic surgery to enlarge the measured signal and the standard frequency signal be counted in the gate time, and these two dynamic scanning count value input in the way the microcontroller AT89S52. AT89S52 P0 port is an 8-bit open drain bidirectional I/O port. As an output port, each pin can drive 8 TTL logic levels. P0 to write "1", the pin is used as a high-impedance input. When accessing external program and data memory, P0 port is also used as the lower 8-bit address / data multiplexed. In this mode, P0 has internal pull up resistor. In the PO port is only used to read external data, so without external pull-up resistor. SCM principle utilization measurement accuracy to calculate the frequency of the signal, and the CPLD gate time is cleared and reset by the MCU control.
4. CPLD implementation module

The system design of measuring frequency range, the relative frequency measurement error for the millionth global standard frequency of 40MHz. If we can achieve accurate count, through simple multiplication and division calculations, you can get the test frequency. However, in the megahertz level count. General microcontroller can not do anything, can CPLD clock frequency up to the nanosecond, can achieve its counting function. On the other hand, to complete the claw above the level of multiplication and division calculation, PLD consume more hardware resources, while the microcontroller almost do not add any cost is not running at the speed limit. Therefore, the use of CPLD and MCU to complete the count complete man-machine dialogue, operation and display.

CPLD internal graphical programming language, programming environment using MAX + plus II complete design documents automatically compile logic, logic simplification, integrated optimization, placement and routing logic, logic simulation, the last of CPLD chip can be programmed to implement the system design requirements.

CPLD internal structure shown in Figure 4 functional modules, including three entities CONTRL, COUNT1 and COUNT2. CONTRL module frequency measurement, test week, self-calibration module selection control, control of the counting means and the measured frequency of the frequency standard, COUNT1, COUNT2 two 24-bit counter, respectively standard frequency and the measured frequency counts, and counting results from the 8-bit bus output to the microcontroller.

The overall waveform simulation as shown in figure 5.

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COUNT is a 24-bit binary counter consists of three 8-bit counter 74393 series components. The difference is that the traditional counter, it uses four 74373 tri-state latches 8 bits of dynamic scan output, COUNT internal structure shown in Figure 6.

COUNT simulation waveform shown in Figure 7.

CONTRL is to achieve a simple data acquisition of logic function, and its internal structure as shown in figure 8.

CONTRL simulation waveform shown in Figure 9, since the CPLD itself there is a time delay (lower latency CPLD chip, the higher the price) is inevitable, so in the gate time count when the measured frequency will be more of a meter when the tip of the pulse, and this will be the tip of the input pulse signal microcontroller, so a microcontroller programming should lose this pulse signal.

5. Conclusion

Accuracy of measurement methods not only has high accuracy, but also remains constant throughout the test precision frequency region. The utilization of precision frequency meter design method, overcomes the disadvantages of conventional frequency measurement principle based on the measurement accuracy of the measured frequency meter with decreased signal frequency reduced. The frequency meter using high-speed CPLD chip to form the main logic module to complete such precision frequency meter master program, designed to achieve a greater frequency range signal frequency measurement.
References

