Design of the pulse spoke measuring instrument

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Abstract

As the high-speed and parallel processing features on FPGA, so it is widely used in high-speed information processing system. In this paper, the front-end data of X - ray energy spectrum is taken as processing object, high-speed data acquisition and processing methods based on the FPGA are proposed, which embodies the advantages of FPGA in the application of high speed information processing. The compensation measures in the electronic measurement system are also discussed in this paper.

Keywords

FPGA; High-speed Information Processing; X-ray energy spectrum; Electronic measurement system; Compensation measures

1. Introduction

The front-end data of X-ray energy spectrum is millivolt voltage pulse sequence, the pulse width of the sequence is microsecond level. But the amplitude and number of the pulse sequence contains the quantitative information of the tested samples [1]. The purpose of the data acquisition and processing system is to extract the pulse amplitude and quantity information from the pulse sequence. The pulse with the same magnitude is classified and summed, then the pulse amplitude information and its corresponding pulse quantity information is transmitted to the host computer for the further processing by serial port. In order to accurately measure the amplitude of the pulse in such a short period， the pulse width is only microsecond level， so the sampled points is not less than 10 during the duration of the pulse. If pulse width is 0.5us, sampling rate should not be less than 20MSPS, such high data streams are not processed by ordinary microprocessors, so the proposed system is FPGA as the control core. The data acquisition and processing system is composed of program control amplifier(PCA), A/D converter, FPGA unit, MCU unit and FIFO interface unit. The system block diagram is shown in figure 1.

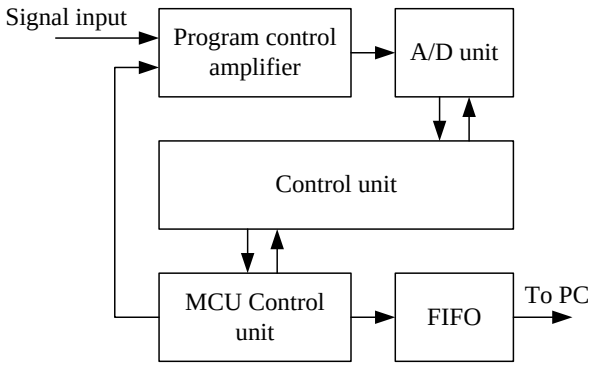

Figure 1 The system block diagram

2. Signal acquisition

The voltage pulse sequence signal is amplified linearly to 0-2V for A/D sampling. For small amplitude and wide bandwidth, the requirement of the amplifier is relatively high, the low noise and broadband is considered.

2.1 The design of programmable amplifier

Programmable amplifier is the key to detect, its stability directly affect the accuracy of detection. The wide bandwidth, high gain and wide dynamic range are the features of the signal amplification part. So two stage amplifiers are adopted, the first stage is 10 times of the fixed amplifier, and the second stage is 1-50 times of the programmed amplification. The first stage is 10 times fixed amplification, and the second stage is 1-50 times programmed amplification, which can realize 10-500 times programmed amplification.The amplifier AD8045 with low noise and high speed operation is selected, whose -3dB bandwidth is 1GHz. The analog switch DG508 is selected, which is controlled by MCU to realize programmed amplification with 8 levels. The principle block diagram of the amplifier is shown in figure 2.

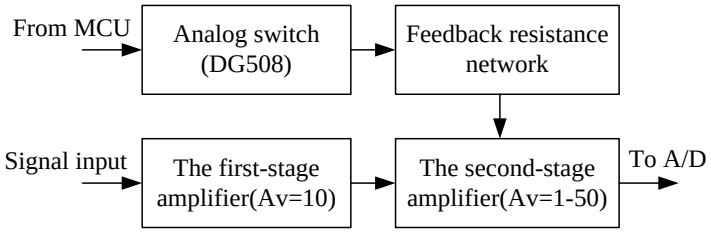

Figure 2 The principle block diagram of the Programmable amplifier

2.2 THE DESIGN OF A/D ACQUISITION CIRCUIT

According to the design requirements for the sampling rate 20MSPS and the resolution 10Bit, analog digital converter AD9224 is selected, whose sampling rate is 40 MSPS and resolution is 12bit, it possess on-chip high performance sample and hold amplifier and reference voltage. Under single + 5V power supply, power consumption is only 376mW. Signal to noise ratio and distortion is + 0.7dB, it have a signal overflow indicator and can directly output data by the binary[2].So AD9224 can fully meet the design requirements. In AD9224, analog input range is very flexible, which can be single or differential input by the DC or AC coupling.AD9224 uses four stage pipeline structure and efficient economic CMOS process is achieves by a broadband input sample and hold amplifier. Signal whose range is 0-2V is input to the AD9224 by a single form, so in AD9224, the reference selection (SENSE) and the reference input (VREF) and the inverted input (VINB) should be connected to the ground. In order to make the sampled data stable, the required precision for the digital power supply and analog power is high, and the filter processing is also very strict, which are obviously different from the low speed A/D design. The specific circuit is shown in figure 3. The clock of Ad9224 is obtained by FPGA dividing, 12 bit parallel data are read into the FPGA on each clock falling edge [3].

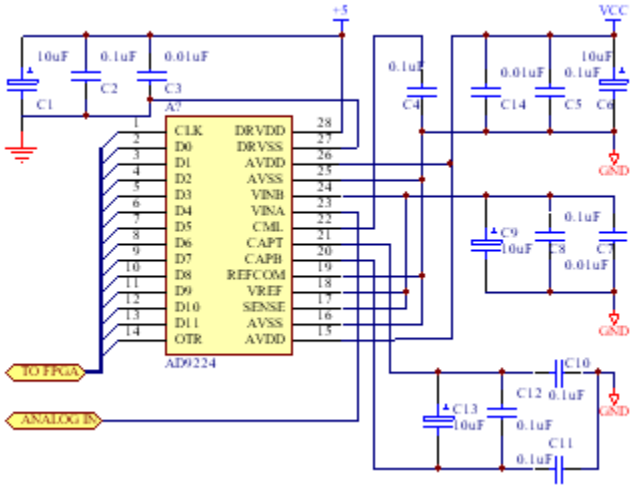

Figure 3 circuit scheme of AD9224

3. The design on the FPGA control unit

Data acquisition and processing are realized by FPGA and the data configuration is achieved by MCU which co-operate FPGA to realize partial low speed data processing.

This design can avoid as far as possible that the FPGA capacity is too large to increase the cost of hardware. According to the design requirements, EPF10K10LC84_4 by Altera company is selected, which is commonly SRAM FPGA including 1000 gates. Because configuration data of the EPF10K10LC84_4 is less than 16KByte, the Flash in MCU can be used to store the configuration data of the FPGA to achieve the configuration of the FPGA [4].

FPGA design is described by MAX+PlusII integrated compiler environment, VHDL hardware description language and schematic input method. The design on FPGA is divided into six units: A/D interface unit, MCU interface unit, sequential control unit, pulse amplitude detection unit, pulse counting unit and data processing unit. The structure relation is shown in Figure 4

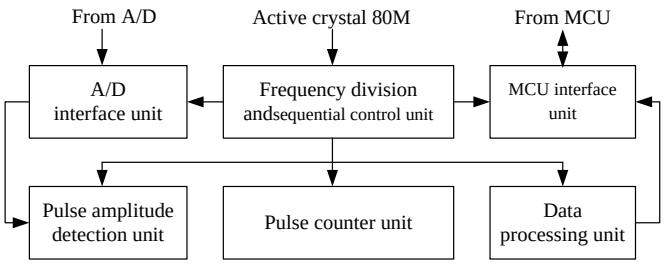

Figure 4 FPGA design principle block diagram

The clock for FPGA is provided by 80MHz active crystal, which is divided 4 frequency as the working clock of A/D converter. When FPGA detects the pulse peak, then begin to read the A/D data, high-speed data flow into the pulse amplitude detection unit for comparison operations and extract the maximum value and the maximum value of two points before and after the data. The data are processed by data processing unit cooperative MCU, and finally the data are uploaded to the host computer. The data exchange of FPGA and MCU is done by MCU interface unit. The interrupt mode is used as data parallel transmission by MCU [5]. The current popular C8051Fx series MCU is adopted in this paper, the specific model is C8051F340, which is 48 pin TQFP package, 64KByte Flash and (4K+256) Byte SRAM memory, the instruction rate up to 48MIPS, integrated with a USB2.0 controller and 1KByte FIFO memory and is very suitable for the design requirements. C8051Fx uses the CIP-51 (8051) core, the instruction system is completely compatible with the 8051, the application scope is very extensive. The uVision2 Keil is used as development environment and the C51is used as the programming language.

4. Compensation measures

Because the dynamic range of the input signal is relatively large, it is necessary to make a nonlinear compensation for the amplifier for ensuring the accuracy of the whole system. The nonlinearity of the amplifier is mainly caused by the change of frequency, amplitude, temperature and so on. The nonlinear error can be compensated by piecewise linear compensation or Lagrange (Lagrange) interpolation. The quantization error is determined by the discrete nature of A/D sampling, which is mainly found in the amplitude of the pulse peak detection. Due to the short pulse duration, the peak amplitude is sharp, and the sampling point can not be guaranteed to overlap with the peak value, which can cause error. Lagrange interpolation measure can be adopted to compensate this error.

4.1 Nonlinear compensation

Nonlinear compensation is common, and the nonlinear compensation measures are discussed in the case of amplitude compensation. The nonlinear error caused by the variation of the input signal amplitude is shown in figure 5 after amplification factor Av is certain.

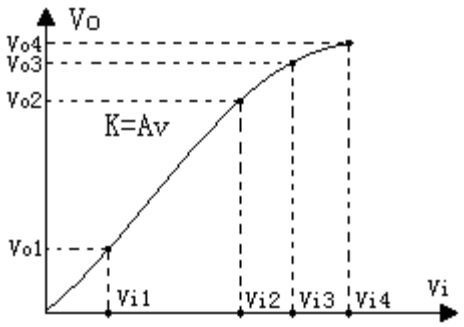

Figure 5 Schematic diagram of amplifier amplitude

Set v_i for the input amplitude, v_o for the output amplitude, $K = Av$ for the voltage amplification factor. With the v_i increase, Av will decrease, the error can be compensated by piecewise linear compensation or subsection Lagrange interpolation based on the practical application. The following is a piecewise linear compensation method, according to figure 5, the input signal can be divided into four sections, including $(0, v_{i1})$, (v_{i1}, v_{i2}), (v_{i2}, v_{i3}), (v_{i3}, v_{i4}) respectively. v_i and v_o can be regarded as linear relation in each segment, and the equation can be written as

$$v_o = Kv_i + B \tag{1}$$

where K and B can be calculated according to the boundary value. The compensation equation is obtained by taking the (v_{i3}, v_{i4}) section as an example.

$$\boldsymbol{v_o} = \frac{\boldsymbol{v_{o2}} - \boldsymbol{v_{o1}}}{\boldsymbol{v_{i2}} - \boldsymbol{v_{i1}}} \boldsymbol{v_i} + \frac{\boldsymbol{v_{i2}}\boldsymbol{v_{o1}} - \boldsymbol{v_{i1}}\boldsymbol{v_{o2}}}{\boldsymbol{v_{i2}} - \boldsymbol{v_{i1}}} \tag{2}$$

This compensation method is simple and the calculation is small, and it is suitable for the occasion where the nonlinear error is small.

4.2 Quantitative compensation

The quantization error is caused by the discontinuity of sampling, as shown in figure 6.This error can be compensated by the Lagrange interpolation method.

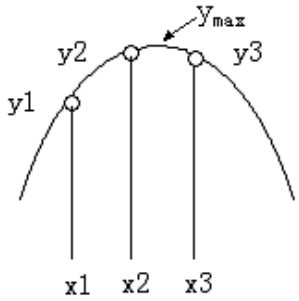

Figure6 The diagram of sampling quantization error

Setting x_1, x_2, x_3 continuous sampling point, the corresponding three sampling points are $y_1, y_2, y_3, y_{\max}$ represents maximum peak value of the pulse, so The two time interpolation expression is

$$y = y_1 \frac{(x-x_2)(x-x_3)}{(x_1-x_2)(x_1-x_3)} + y_2 \frac{(x-x_1)(x-x_3)}{(x_2-x_1)(x_2-x_3)} + y_3 \frac{(x-x_1)(x-x_2)}{(x_3-x_1)(x_3-x_2)} \tag{3}$$

When $x_1 = -1$, $x_2 = 0$, $x_3 = 1$

$$y = (0.5y_1 - y_2 + 0.5y_3)x^2 + (-0.5y_1 + 0.5y_3)x + y_2 \tag{4}$$

$$y_{\max} = \frac{4ac - b^2}{4a} = y_2 + \frac{(y_1 - y_3)^2}{8(2y_2 - y_1 - y_3)} \tag{5}$$

Lagrange interpolation is applied widely in engineering, and it has a high fitting precision. But the computation is large, and it is suitable for the occasion of high nonlinear error and high precision.

5. Conclusion

In this system, FPGA is used as the main controller for high-speed data acquisition and processing, and the FPGA data configuration and auxiliary calculation of partial data is carried by the MCU. Low noise high-speed operational amplifier AD8045 can achieve the 10-500 programmable amplifier and the gain bandwidth can reach 0.5G. High-speed A/D converter AD9224 can achieve the pulse signal sampling and the sampling rate reached 20MSPS. The system uses a variety of anti-jamming measures to achieve the stability of the system, using a variety of compensation measures to ensure the accuracy of the measurement. By testing, the system has achieved the design requirements.

Reference

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