A high resolution FPGA based time-to-digital converter

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Abstract

A high resolution Time to Digital Converter (TDC) with Virtex-5 Field-Programmable Gate Array (FPGA) ML507 device is proposed. The MUXCY block of the CARRY4 in FPGA is used to design the tapped delay line. A two-stage data flip-flop (DFF) array data latching structure was designed to avoid the metastable states. An improved thermometer code encoder method is proposed to reduce the measurement errors. The code density test calibration is used to eliminate the RMS. The simulation results show that the TDC's average least significant bit (LSB) is 14.49ps, the TDC's Differential Non-Linearity (DNL) is less than 5.4LSB and Integral Non-Linearity (INL) is less than 12LSB. Without the Ultra Wide Bin (UWB), the TDC's measurement error was less than 30ps.

Keywords

Time to Digital Converter (TDC), FPGA, Virtex-5, high resolution.

1. Introduction

Time to digital converter (TDC) is used for precise time interval measurement. Usually, it can achieve a resolution of nanosecond even picosecond level at a relative low clock frequency. It is widely used in scientific experiments and engineering applications, such as Positron emission (PET) experiment [1], laser-range-finder system [2] and so on.

There are mainly two types of TDC. One is ASIC-TDC and the other is FPGA-TDC. Though ASIC-TDC has excellent performance, its disadvantage is long design cycle, high-cost, complexity and poor flexibility. FPGA-TDC can achieve a better performance as well, and in the meantime, it has the advantage such as short design cycle and good flexibility.

The most common way to design the FPGA-TDC is time interpolation. It includes tapped delay line TDC, phase-shift clock TDC, the vernier TDC and so on. Tapped delay line is the most popular structure, and it can achieve a high resolution of few tens picoseconds [3-6]. There are many ways to improve the resolution of tapped delay line TDC.

In 2008, J. Wu and Z. Shi, et al [7] present a wave union method to further improve the resolution. The logical cell which can be easily cascaded as basic delay element can be used to improve the resolution as well. In recent years, inverters [5] have been replaced by carry logics using as delay element. M. Büchele, H. Fischer et al using phase-shift clock method achieved 160ps resolution in Xilinx Virtex-5 devices [8]. Other methods mainly used in ASIC-TDC, also have been proved useful in FPGA-TDC design. In 2009, A.M. Amiri et al [9] using Vernier method achieved 75ps resolution in FPGA. In 2010, R. Szplet and K. Klepacki [10] providing a new approach to design FPGA-TDC, they implement a pulse shrinking TDC in FPGA.

In this paper, a tapped delay line TDC is designed on Xilinx Viretx-5 ML507 device. In the following section, we present the architecture of TDC and the characteristic of tapped delay line. In section 3, the improved thermometer code encoder is proposed to reduce the measurement errors. In section 4, the

code density bin by bin calibration method is discussed. In section5, the experiment results are discussed. In section 6, the conclusion is got.

2. TDC Architecture

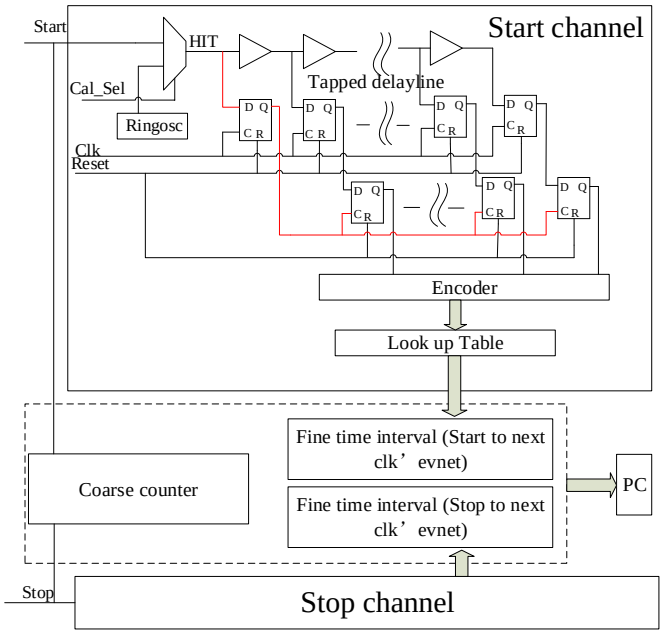
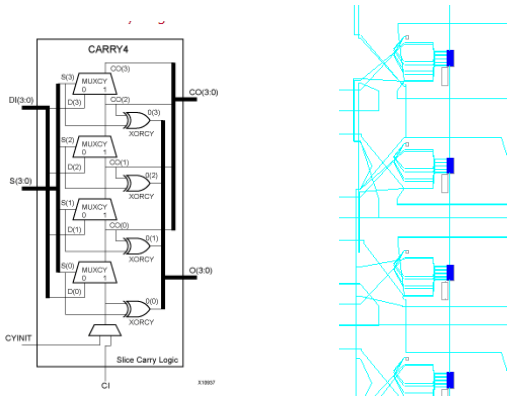


Fig 1 Block diagram of the Time-to-Digital Converter



(a) CARRY4 (b) Dealy line in FPGA

Fig.2. The delay element in FPGA

The architecture of the proposed TDC circuit is shown in Fig.1. There are two fine measurement channels and a coarse counter to measure the time interval between the start signal and stop signal. Each channel is mainly consisted of tapped delay line, DFF (Data Flip-Flop) arrays, encoder circuit, lookup table and ring oscillator.

A counter is used for coarse time measurement and tapped delay line for fine time measurement. The fine time measurement means to calculate the time interval between HIT event and the next clk'event. The two channels (start channel and stop channel) is designed to perform the fine time measurement. The two stage DFF arrays is used to latch the signal from the tapped delay line. The signal is latched on the rising edge of clock and the data are stored as thermometer code. The input signal of the first stage DFF array's clock port is system clock which is also used for coarse measurement. As marked with red color in Fig1, the input signal of the clock port in second stage DFF array is the output of the first stage of DFF, in which, the Hit signal is latched directly without any other delay elements. Two stage DFF

arrays can avoid the propagation of metastable state and convenient the data flow control. The ring oscillator is used for code density test calibration, and the look up table stores the calibration results.

The tapped delay line is built by CARRY4 in our design. The internal architecture of CARRY4 is shown in Fig 2(a), each CARRY4 has four MUXCYs. The MUXCY is used as a basic delay element and the signal from the output port of CO(3：0) can be latched with the DFF array. Then the CARRY4 can be divided into four taps. After placed and routed by XILINX FGPA Editor software, the delay elements were cascaded together. Thus reduced the routing path between two adjacent CARRYs and then reduced the delay time between two delay elements.

3. Encoder module

Encoder circuit is used to transform the thermometer code to binary code that will be conveniently stored and operation. Dichotomous search algorithm is usually used for transforming thermometer code to binary code. The delay line built with CARRY4s is not a ideal delay line, this is due to the fast look ahead circuit in the CARRY4 block. The simulation result shows that the delay time of the output signal is disordered (Fig3). For example, if the current state is (111111110101) then next state will be (111111111101). If the encoder circuit can't distinguish the difference between two states, some states may never appear in the encoder result. However, one thing we will be sure is that the number of 1 is directly proportional to the length of time interval, so the tapped delay line can still be used for fine measurement. The dichotomous search algorithm will be improved to adapt the fake thermometer code.

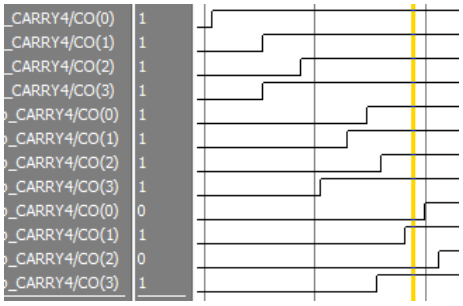


Fig 3 Timing analysis after place and route

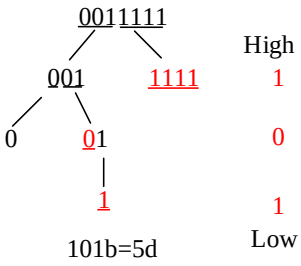


Fig 4 Thermometer code encode principle

Dichotomous search algorithm is used to count the number of continuous 1 and then the following four bit are added one by one. The dichotomous search algorithm is improved as following. As shown in Fig4, the 7 bits thermometer code is used to illustrate how it transformed into 3 bit binary code. First, the last four less significant bits and not just only the 4th bit is checked, if they were all 1, we can conclude that the 2th bit of binary code should be 1, then the high 3 bits is split into two parts to check and so on. If not, the 2th bit of binary code should be 0, then split the low 3 bits to check and so on. By this way, the encoder circuit can calculate the number of continuous 1 in N bits thermometer code by $\log_2 N$ steps.

4. Calibration module

Influenced by PVT (Process, Voltage Temperature), the delay time of each delay element will be different. In order to get accurate measure result, the delay line will be needed to be calibrated before

measurement. The code density test is used to calibrate the tapped delay line. Code density is a bin by bin calibrate method.

The principle of the code density test is shown in Fig5. There is no correlation between Hit signal and Clk signal. That means the probability of Hit signal hit the Clk within a cycle at any point were equal. Assuming that, in N tests the number of M appears k times in the encoder result. Then we can conclude that the delay time of Bin_M (t_M) can be written as

$$t_M = \frac{k}{N} T \tag{1}$$

Where, T is the cycle time of Clk. By using this method, we can calculate the delay time of each delay element.

Then the fine measurement result t_{fc} can be written as

$$t_{fc} = \sum_{i=0}^{M} t_i \tag{2}$$

where M is the encoder result.

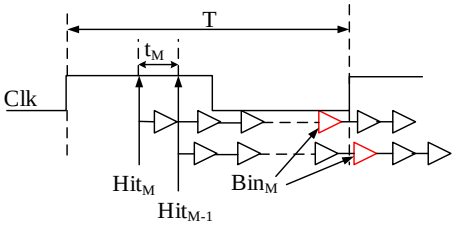


Fig 5 Code density test principle

The problem is how to generate the Hit signals which have no correlation with the system clock Clk. The general method is with a ring oscillator. In reference [4], the odd numbers of inverters is used to generate the hit signals. In this design, the LUTs is instead of inverters to generate the hit signals, this is due to there are much of LUTs resources in Virtex-5 device.

5. Results and discussion

5.1 Measurement precision

The delay time of each delay element is shown in Fig.8. The Hit signal stop at tap (345), that means the average lest significant bit (LSB) was about 14.49ps (5000/345).

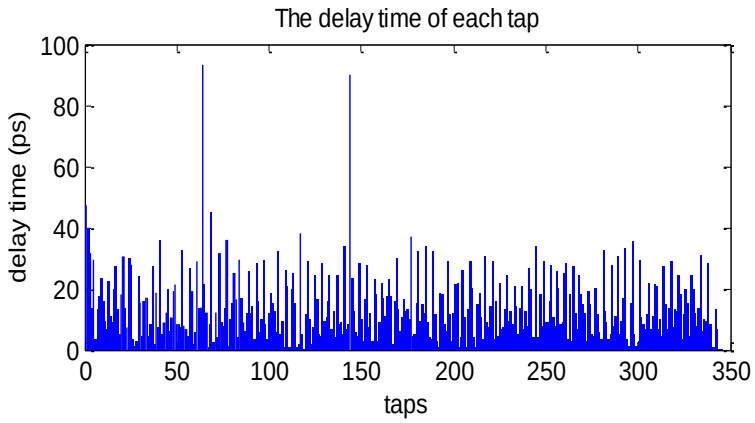


Fig 6 Delay time of each delay element

It is also obviously to see that the delay time of the most of the delay elements are less than 40ps, but there were two elements' delay time much longer than other elements and almost reached 100ps, which is called Ultra Wide Bin (UWB) [7]. The wave union method can solve this problem, but its encoding method is very complicated. There are only several of UWBs, it is not worth to use wave union in our design. Because the measurement is calibrated bin by bin, so the measurement error was determined by

the last bin 1 where DFF array latched. For this reason, we mark the two UWBs, and compare the measuring result with UWBs after each measurement, if they were equal then restart the measurement to avoid the big measurement error. With this method, the measurement error can be reduced to about 30ps.

Summary the delay time of each delay element, a histogram is built as shown in Fig.7. The histogram can be stored in the LUTs of the FPGA device. We can get the fine measurement time interval from the LUTs based on the encoder result. The LUTs should be refreshed after each time of calibration.

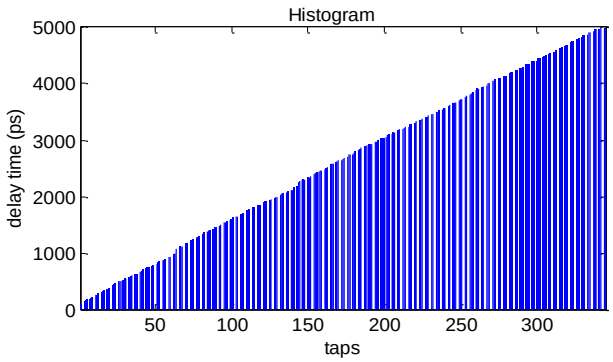


Fig 7 Histogram of delay line

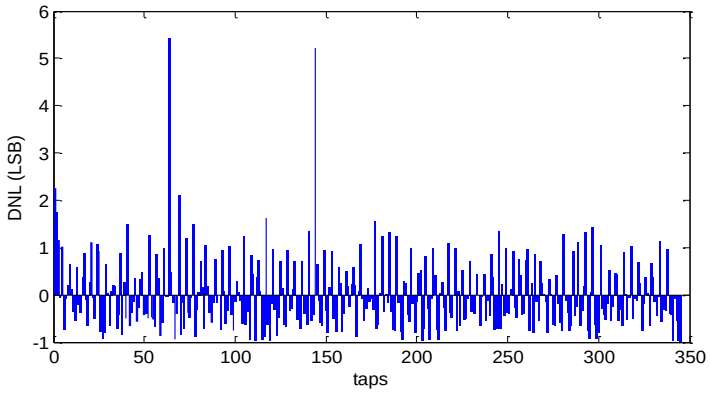


Fig 8 The DNL of tapped delay line

5.2 DNL and INL

The Differential Non-Linearity(DNL) of tapped delay line is shown in Fig 10, the DNL's range was about (-0.1 ,5.4) LSB. The DNL's range will be narrowed down to (-0.1, 2.2) LSB except of two UWBs.

The Integral Non-Linearity (INL) of tapped delay line is shown in Fig 9. It can be seen that the INL was ranged from 0 to 12 LSB.As shown in Fig10, compared with the real delay time is a little above the ideal delay time, that is consistent with the INL analysis.

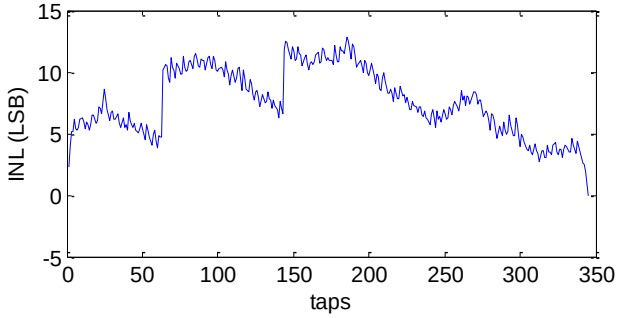


Fig 9 The INL of tapped delay line

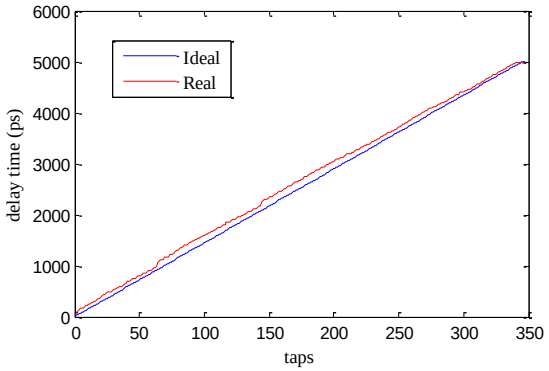


Fig 10 Ideal and Real delay time

6. Conclusion

A high resolution (14.49ps) TDC circuit with tapped delay line is implement on Xilinx Virtex-5 ML507 development board. The tapped delay line was built by chained CARR4s. A new data latching method for tapped delay line structure TDC. In order to adapt to the CARRY4's features, the encoding method is improved to compute the thermometer code with few disordered bins. With code density test calibration, the TDC's resolution on average approaches 14.49ps. The TDC's DNL is 5.4 LSB and INL is 12 LSB. The measurement errors caused by UWB is greatly reduced to about 30 ps.

Reference

[1] B.K. Swann, B.J. Blalock et al.: A 100-ps time-resolution CMOS time-to-digital converter for positron emission tomography imaging applications, IEEE J. Solid-State Circuits, vol.39(2004): p.1839–1852

[2] P. Palojarvi, K. Maatta, J. Kostamovaara.: Integrated time-of-flight laser radar. IEEE Trans. Instrum. Meas, vol.46(1997),p. 996–999

[3] L. Zhao, X. Hu.: The Design of a 16-Channel 15 ps TDC Implemented in a 65 nm FPGA, IEEE Trans. Nuclear science.vol.60(2013),p. 3532 – 3536

[4] J. Torres, A. Aguilar.: Time-to-Digital Converter Based on FPGA with Multiple Channel Capability, IEEE Trans. Nuclear science.vol.61(2014),p. 107 - 114

[5] M.W. Fishburn and L. H. Menninga, A 19.6 ps FPGA-Based TDC With Multiple Channels for Open Source Applications, IEEE Trans. nuclear science.vol.60(2013),p.2203-2208

[6] W. Pan, G. Gong, and J. Li.: A 20-ps Time-to-Digital Converter (TDC) implemented in Field-Programmable Gate Array (FPGA) with Automatic Temperature Correction, IEEE Trans. nuclear science. vol.61(2014), p.1468-1473

[7] J. Wu and Z. Shi.: The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay, in Proc. IEEE Nuclear Science Symp.(2008) p. 3440–3446

[8] M. Büchele, H. Fischer, M. Gorzellik, et al., A 128-channel Time-to-Digital Converter (TDC) inside a Virtex-5 FPGA on the GANDALF module, J. Instrumentation. vol.37(2012),p. 1827–1834

[9] A. M. Amiri, M. Boukadoum, and A. Khouas.: A Multi-hit Time-to-Digital Converter Architecture on FPGA, IEEE Trans Instrumentation and Measurement. vol.58(2009), p.530—540

[10] R. Szplet and K. Klepacki.: An FPGA-Integrated Time-to-Digital Converter Based on Two-Stage Pulse Shrinking. IEEE Trans. instrumentation and measurement. vol.59(2010), p.1663-1670