Avalanche Photodiode Fabricated in Standard 0.35 μm CMOS Process

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Abstract

We present a structure and equivalent circuit model of avalanche photodidode with standard 0.35-μm complementary metal-oxide-semiconductor (CMOS) technology. Measurements demonstrate that this structure offers a high dynamic responsivity and a high frequence The equivalent circuit model of CMOS APD include several components that provides accurate impedance characteristics and parasitic effects.

Keywords

Avalanche photodetector, 0.35μm CMOS, equivalent circuit

1. Introduction

Short-distance optical communication includes fiber-to-the-home(FTTP) and chip-to-chip and other applications of high speed data transmissions, Si photodiodes (PDs) are used widely due to its low power consumption and low cost. Avalanche photodiode (APD) is the critical of photodiodes, because of a strong internal gain and a high bandwidth. APD fabricated with 0.35μm CMOS process ensure other electronic circuits integration with optical devices for easy without any process violation, and mostly used in optical interconnection applications [1]. One big challenge of CMOS-APD is that the small quantum efficiency and bandwidth of the product. The absorption length of silicon at 850 nm is as much length as the N-well [2] .consequently, the incident photons absorbed in the P-substrate region generate carriers and transportation speed is very slow.

2. Stucture of CMOS-APD

2.1 Structure

Figure 1 shows typical structure of the CMOS-APD.In our sructure of CMOS APD,. P+/N-well junction for detection of photo was presented. In the P+/N-well junction junction, The time that most of photo-generated carriers diffusion in the N-well region is small due to the thinner length of N-well region [3]. We also pursued a different junction to eliminate photo-generated carriers in the P-sub region.to P+/N-well junction,because of the slow diffusion speed in the P-sub.This is N-well/P-sub junction,which has been used widely in almost CMOS APD structure. However, CMOS APD having P+/N-well junction suffers from a disanvantage due to low responsivity by the reduced length of N-well.

2.2 Characterization

Figure 2 shows the I-V characteristics of the CMOS-APD. The dark current is very small The value is about 10^{-13} at a low bias.We can discover that when the bias voltage is above 9 V,the light current increased gradually ,therefore the breakdown voltage of CMOS APD is 9.3 V. At the same time, the

conditon of light illumination is that the wavelength (λ)=830 nmand the light power (P)=10 μW.We also find in the picture that the responsivity of CMOS-APD is 0.95A/W.

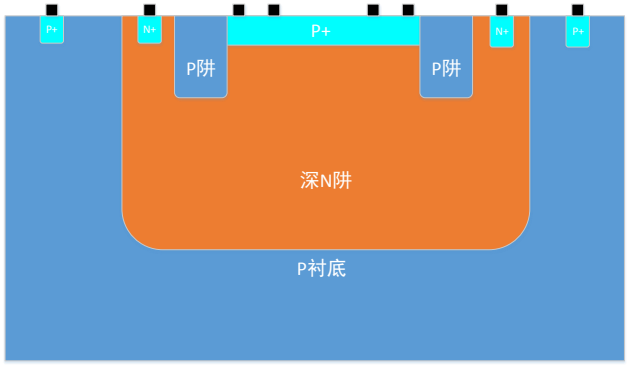

Fig. 1. Cross-sectional view of P+/NWELL CMOS-APDS

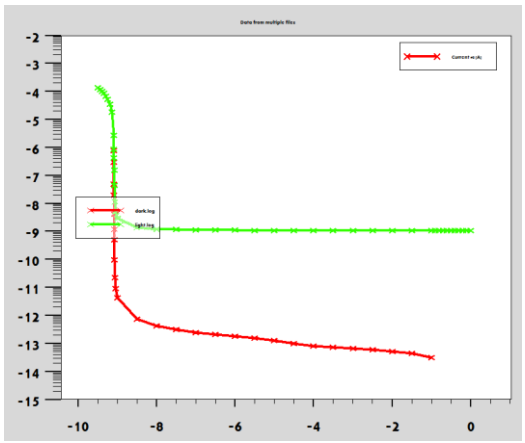

Fig. 2. I-V characteristics of the CMOS-APD

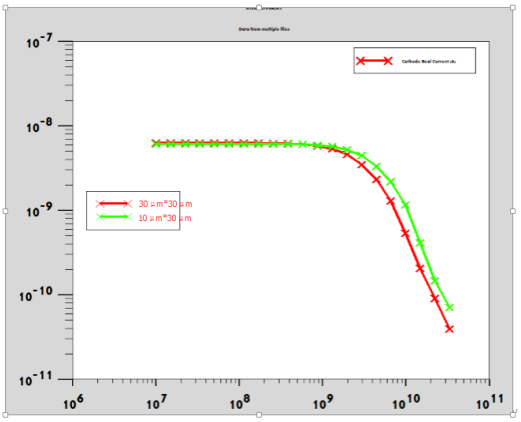

Fig3 Frequency response of CMOS-APD

In CMOS-APD, there are two factors that limited the photodiodes bandwidth. One is diffusion time that photo-generated carriers in N-well region; the second is the RC time constant of P+/N-well junction [4]. Among these, the diffusion time is not easy to decrease in the standard CMOS process as it need to violate the design rule of CMOS process. but we provides smaller junction capacitance to reduce the RC time constant by the PD area reduction, We have investigate a CMOS-APD in our previous report ,which the optical-window area of CMOS APD is about 30 μm × 30 μm [5], but we use a CMOS-APD which the optical window area is about 10 μm × 10 μm in our present report.

Fig. 3 shows the photodiodes frequency responses of CMOSAPD with different optical window areas. When the optical-window area increased, the photodiodes response decreased due to increased RC time constant. For the optical-window area of CMOS-APD is 30 μm × 30 μm, the 3-dB bandwidth at the breakdown voltage is about 3.7GHz. For smaller CMOS-APD, the 3-dB bandwidth is about 6.3

GHz...Consequently, the smaller area of optical-window that the frequency of CMOS APD is increased.

3. Model of CMOS-APD

3.1 Model of P+/N-well junction

Fig. 4 represents the circuit model for P+/N-well junction. This structure is a one-sided abrupt P+/N-well junction. Research show that there are the avalanche,and drift region in the depletion layer of junction.the avalanche region of P+/N junction is modeled as a shunt combination of an inductor and a capacitor [6]. the ac conduction current in the avalanche varies inversely with ω,Thus, impedance of P+/N−well includes an inductance .So La given as

$$L_a = \tau_a / (2\alpha' I_0) \quad (1)$$

Where α' is the derivative of the ionization coefficient.but the coefficient is relating to the electric field, τ_a is the transit time of carrier from N-well to P+-layer, and I_0 is the bias current[7]. Also the capacitance of P+/N-well junction in the depletion layer of junction is $C = \varepsilon A / W_D$, and the resistance in the depletion layer of P+/N−well is that $R_d = W_d / 2A\varepsilon v_S$, where ε is permittivity in the silicon , A is the optical-window area of , W_D is length of the layer of junction, W_d is width in the drift region, and v_S is the velocity of carriers in the drift region [8]. the equivalent circuit model also included R_a and R_1, series and parallel resistors,. R_S represents the inactive region resistance in the low doped N-well

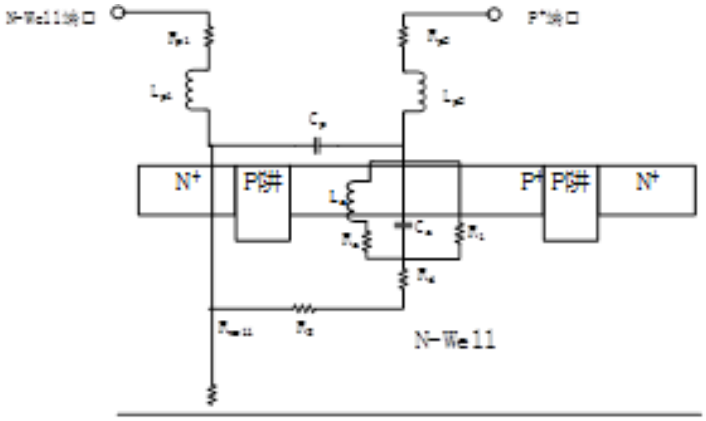

Fig4 Model of P+/NWELL junction

3.2 Model of pad

Fig5 show that the circuit model for and interconnection lines and pad In the equivalent circuit model ,C_{pad1} represents the capacitance in the P+layer , and C_{pad2} and R_{pad1} are caused by leakages cureent in the pad. R_{pad2} and L_{pad} are the parasitic resistance and inductance.

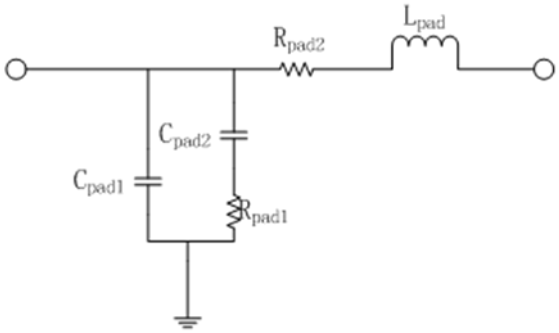

Fig5 Model of Pad

3.3 Model of N-well/P-sub junction

Fig6 show that the circuit model for N-well/P-substrate junction, where C_{sub1} is the capacitance in the depletion layer of N-well/P-sub, and C_{sub2} and R_{sub} are represent the parasitic effects of Si P-substrate.

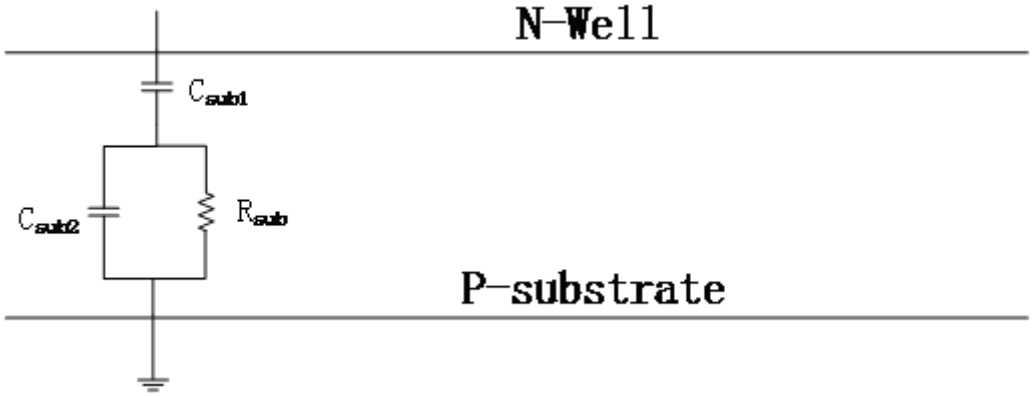

Fig6 Model of N-well/P-sub junction

4. Conclusion

In this paper, we have demonstrated structure and equivalent circuit model avalanche photodiodes with standard 0.35μm complementary metal-oxide-semiconductor (CMOS) technology. The maximum bandwidth of 7GHz is achieved at the responsivity of 1 A/W. The equivalent circuit model of CMOS-APD also have been presented.

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