Design of BiFET stacked folded differential Power Amplifier for TD-LTE

Wei Wang [a], Wenqi Cai, Xiao Mo and Feng Hu

School of Electronics Engineering, Chongqing University of Posts and Telecommunications, Chongqing 400065, China

[a]747169108@qq.com

Abstract

This paper presents a RF power amplifier(PA) designed for the TD-LTE standard.The power amplifier is based on the Stacked Folded Differential structure.The first stage is a differential common-source amplifier, which is used to amplify the signal from the input matching .And the second stage is a BiFET Stacked Folded Differential amplifier which is used as main power amplifier to improve the linearity. The proposed PA is designed with Jazz's 0.18 um SiGe BiCMOS technology, The simulation results with Spectre RF show that the PA achieved a Gain of 32 dB, a P1dB of 29 dBm. Within the operating frequency rage of 2.5-2.7 GHZ, the PA has an S11 and S22 below -10dB, and the peak PAE is 22.1%.

Keywords

RF PA; BiFET ; Stacked.

1. Introduction

In order to meet the requirements of high data rate, the fourth generation(4G) wireless communication systems has been rapidly increasing. And the power amplifier is very important part in 4G wireless communication systems.Especially its performance,such as linearity and PAE,is critical to the performance of the whole system performance. In the past for a long time,power amplifiers have basically been done by expensive technologies such as GaAs,to achieve excellent performance[1]. However,in recent years, with the rapid development of the mobile communication technology, SiGe BiCMOS technology has a wider range of application in power amplifier.Because SiGe BiCMOS technology made it easy to integrate a PA with an intelligent control circuit.In addition,the cost of silicon chip is less than that of CaAs or InP[2],from the financial perspective. This paper designed a tow-stage power amplifier at 2.6 GHZ center frequency for TD-LTE application.The simulation results with Spectre RF show that the PA achieved a Gain of 32 dB, a P1dB of 29 dBm. Within the operating frequency rage of 2.3-2.7 GHZ, the PA has an S11 and S22 below -10dB, and the peak PAE is 23%.

2. Design considerations

The SiGe power amplifier consists of a tow-stage amplifier with input, inter-stage, and output mathing networks and tow bias circuit.Fig.1 shows the Block diagram of the PA.

The first stage is a differential common-source amplifier, which is used to amplify the signal from the input matching .And the second stage is a BiFET Stacked Folded Differential amplifier which is used as main power amplifier to improve the linearity. Fig. 2 shows the Schematic of the power stage.

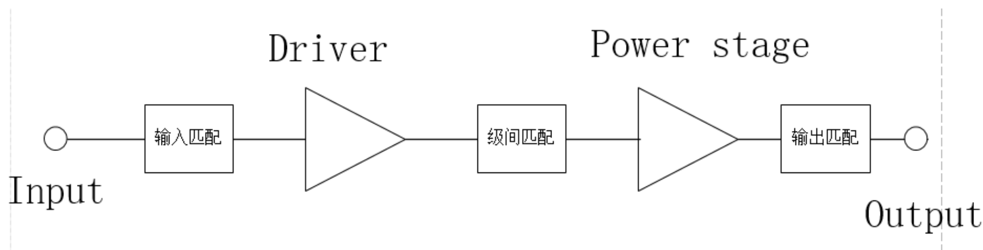


Fig.1 Block diagram of the PA

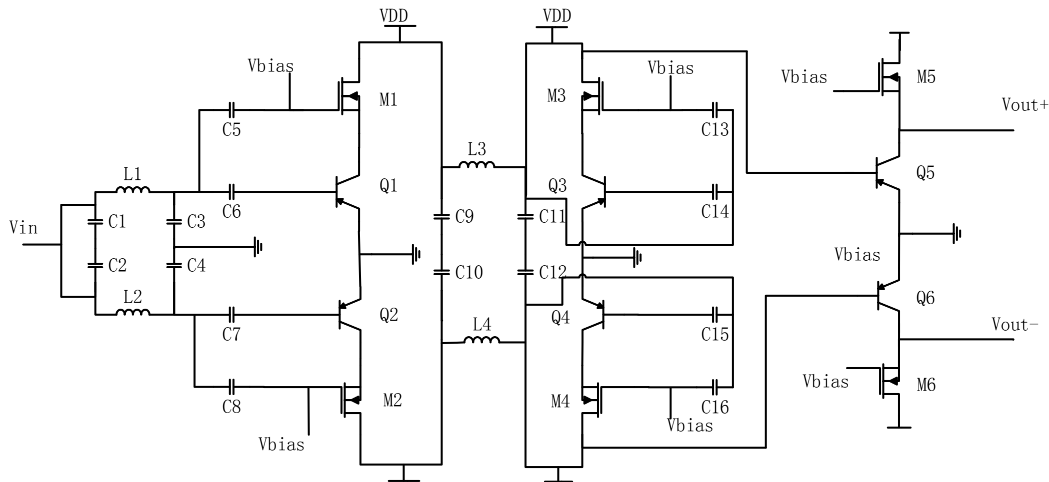


Fig.2 Schematic of power stage circuit

2.1 BiFET configuration

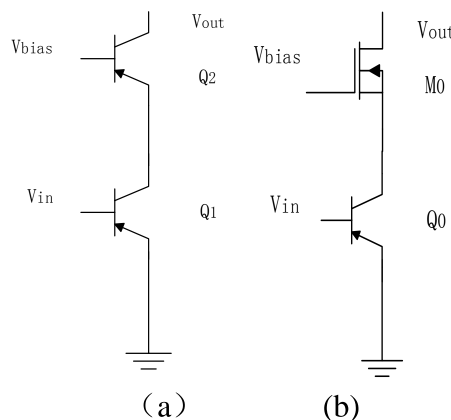
The With the development of the RF technology, a variety of PA configurations are in use today. The cascode is the most popular one among them. The traditional cascode structure is widely used in wireless applications because of its simple configuration, low power consumption and high gain.[3]

As the Fig.3 (a) shows, the voltage gain of the cascoded PA can be obtained as:

$$A_V = -g_m \bullet Z_L \tag{1}$$

The'gm' is the trans conductance of the bipolar. Usually the'gm' of the bipolar is larger than that of MOSFET.

Fig.3 (b) shows the BIFET structure circuit.In order to meet high linearity, The output stage M0 adopts MOSFET. And the input stage using bipolar transistors, to ensure a high gain and low noise.[4]



（a） (b)

Fig.3 BJT structure and BIFET structure circuit

The BJT cascode amplifier and the BiFET amplifier circuit are shown in Fig.3.Under same conditions of supply voltage, the simulated results of P1dB are shown in Fig.5.It can be seen from the figure, the BiFET structure circuit has a better linearity compared with the traditional cascode circuit.

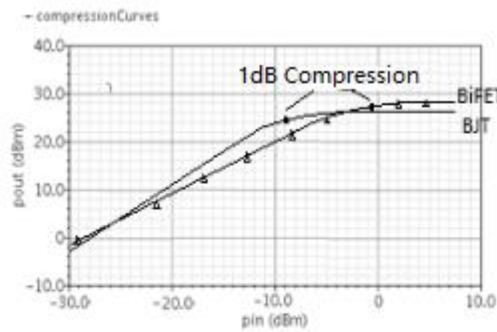


Fig.5 Simulated results of P1dB of traditional cascode and BiFET structure circuit

2.2 Stacked folded differential PA structure.

Fig.6 shows the stacked folded differential PA structure circuit. C1 and C2 capacitors are used for coupling. The input power is applied to M1 and M2 .Do not need specific transistor to complete phase shift. The Pout of a traditional differential structure is limited by the breakdown voltage of transistor M2.However, in stacked folded differential PA structure, M1 is stacked, to increases the total output shift.In addition, compared with traditional differential pairs,it has a better linearity.[5]

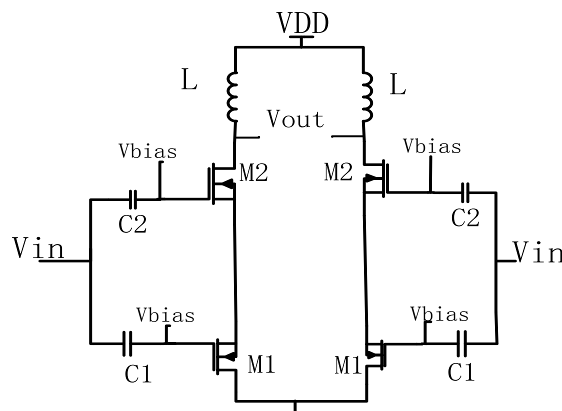


Fig. 6 SFDS PA structure

Fig.7 shows the half circuit of stacked folded differential structure and the voltage Waveform of MOSFET. Contrary to a traditional cascode differential circuit, M1 and M2 can have different gate thickness. Hence, the linearity of stacked folded differential structure is improved by using a thicker gate oxide of M2 to sustain a high voltage exhibiting good linearity performance.[6]

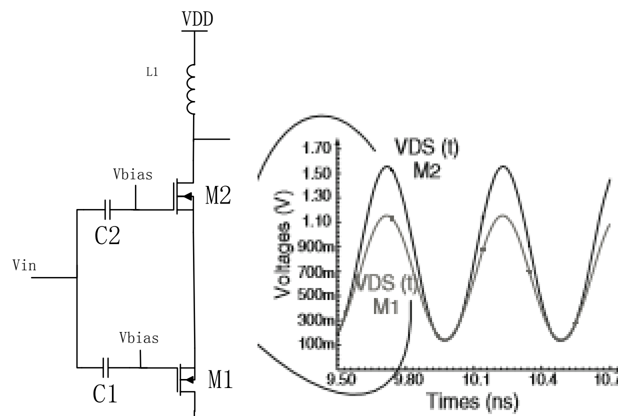


Fig. 7 half circuit of stacked folded differential structure and the voltage Waveform of MOSFET

Increasing the size of M2 can enhancing linearity. However, the reliability of the circuit is deteriorated when the size of M2 increases significantly compared to M1,[7]Therefore, The difference between M1 and M2 must be reasonably controlled, to maintain good linearity. Meanwhile, avoid the risk caused by the decline of stability.

3. Simulated results

The proposed PA is designed with Jazz's 0.18 um SiGe BiCMOS technology, the supply voltage is 3.3 V. The layout of the core circuit is shown in Fig.8.And the layout of the circuit occupancy area: 0.7116*2.1313=1.61851mm^2

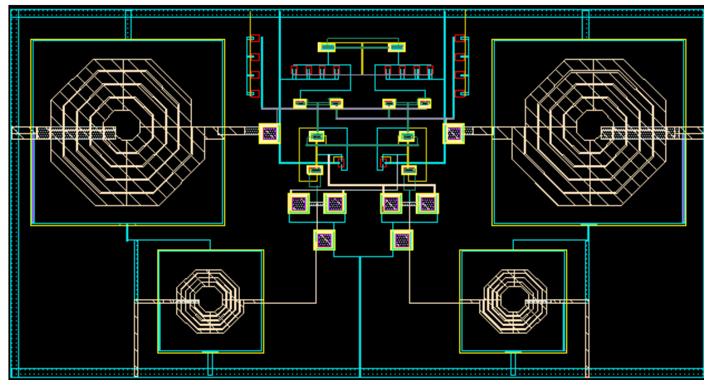


Fig.8 The layout of this PA

the parameter S11, S22were measured and shown in Fig. 9 .It shows that in the band of 2.5-2.7GHZ,S11<-10dBm,S22<-10dBm.

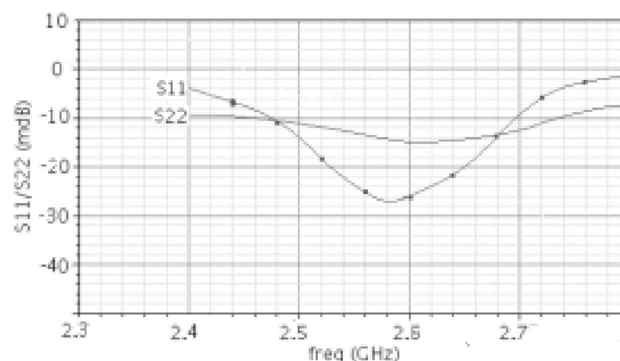


Fig. 9 Simulated results of S11 and S22

The gain is a very important indicator in LTE PA.PAs need sufficient gain to let linear power output no fewer than 26dBm. Fig. 10 shows a plot of measured gain, and Fig.11shows the simulated result of PAE. We can perceived from the diagram, that the maximum output power gain is 32dB and the maximum PAE value is 23%.

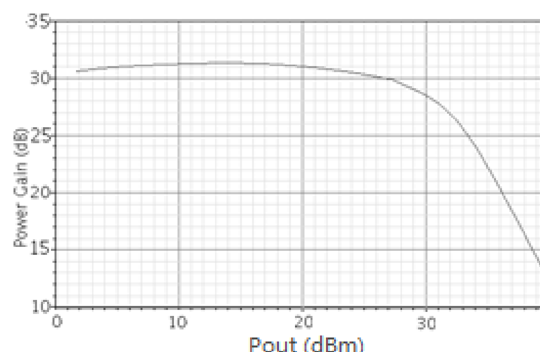


Fig.10 Simulated results of Power Gain

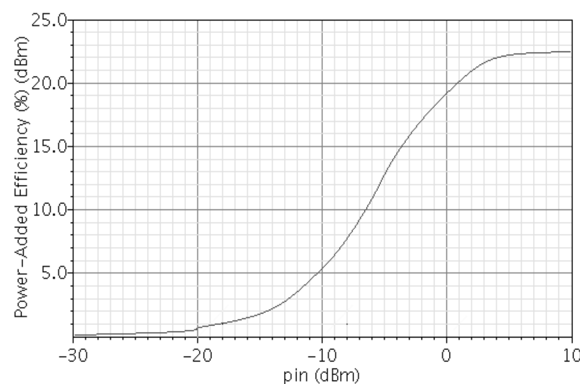


Fig.11 Simulated results of PAE

The summary of LTE PA performance is given in Table 1 [8]-[11]

Table 1 The summary of LTE PA performance.

Ref.	center	technology	Linear output	gain	PAE
	[GHz]		[dBm]	[dB]	[%]
This work	2.6	0.18um BiCMOS	29.54	32	23
[8]	2.4	0.18um BiCMOS	23	27.3	21.3
[9]	2.4	0.18um CMOS	26	30.6	26.7
[10]	2.5	0.18um CMOS	-	28	21.2
[11]	1.85	0.18um BiCMOS	20.4	30.5	22

4. Conclusion

This paper designed a tow-stage power amplifier at 2.6 GHZ center frequency for TD-LTE application. The simulation results with Spectre RF show that the PA achieved a Gain of 32 dB, a P1dB of 29 dBm, a PAE of 23%. Within the operating frequency rage of 2.5-2.7 GHZ, the PA has an S11 and S22 below -10dB.

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