Research and design of low phase noise of PLL frequency hopping source in modern microwave

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Abstract

With the rapid development of the modern telecommunication and radar electronic reconnaissance and countermeasure technology as a core component of the frequency synthesizer performance put forward higher requirements， Especially phase noise performance of PLL frequency synthesizer, as the mainstream of modern frequency synthesizer of the synthesis technique of low phase noise is very necessary in this paper based on the of phase-locked loop with low phase noise theory and design research and analysis.The main purpose of this paper is to study the modern microwave PLL frequency source with low phase noise design technology of phase locked loop based on noise performance analysis and methods for low phase noise design of modern microwave PLL frequency hopping from a variety of sources of an analytical study is presented for the design of low noise PLL frequency source of some unique insights into the first of the modern frequency synthesis technology of is followed by a detailed analysis of the phase locked loop components of PLL noise contributions include loop filter noise effects resulting in a more accurate phase noise prediction algorithm in addition of Fractional-N PLL this with breakthrough synthesis technique for the analysis in this,The last part of the paper the several low noise of PLL frequency synthesizer design example design theory of low noise PLL frequency source for validation and achieved a very high phase noise performance has certain guiding significance and reference value.

Keywords

Phase locked loop phase noise loop filter frequency hopping source.

1. frequency and frequency synthesis

Frequency synthesizer is by one or several reference frequency produced one or many frequency output a high quality signal generator frequency synthesis technology originated in the 1930s to now has 70 years of history as electronic system of the core parts in electronic technology and other areas have very extensive use of special application in the field of radar electronic guided weapons against electronic mobile communication electronic measurement is widely.Due to the direct frequency rate of synthesis technology with many different frequency rate into the double line frequency divider and frequency doubling output frequency clutter interference is very large and body product and circuit design more complex it can't adapt the modern electronic equipment of frequency source with high frequency spectrum purity and the requirements to produce the rate of the second generation of frequency synthesis is connected frequency rate of synthesis device is modern phase locked frequency synthesis device.With the digital signal of the computer technology, DSP technology and micro electronic technology development in the frequency domain as the birth of a revolutionary technology that is in 1970s the DDS (Direct Digital Synthesis) direct digital frequency synthesis DDS is 70 years at the beginning of the United States J.TirneyC.M.Radar and B.Gold proposed by DDS with ultra high speed agility (<0.1 s), ultra fine resolution (up to 1 Hz) variable frequency phase continuously to output signal

is easy to realize linear frequency modulation and other various frequency, phase, amplitude modulation and digital to set a superiority to the short period of twenty years has been rapid development and Spurious of DDS AD9854, such as on the widely used it in terms of radar electronic anti military aspects in nuclear magnetic resonance of civilian electricity is waving a huge role but the DDS has two obvious not enough of the DDS output frequency band limited actual most high output frequency only reference clock 40 left and right clock frequency is 300 MHz with actual output bandwidth of 120mhz due to the phase truncation amplitude measurement and digital to analog converter of the non ideal characteristics and leads to the very rich which are seriously restricted the DDS greater scope of application.

First on the lower surface of the sea and in recent more than ten years electronic technology development speed surprised people by the development of the electronic equipment especially is no line electric communication radar air navigation and deep space detection technology and equipment of technology more and more to be in more and more high the frequency synthesis device and index also provided a more high requirements also stimulated the frequency synthesizer into a step development using PLL device as an example to see the frequency synthesis technology development status of frequency synthesis device chip the technical indexes greatly improve.

2. The basic theory and the theory of phase locked loop

The phase locked loop is a phase - level self - control system, which is composed of three parts： Phase detector, PD loop filter, LF voltage controlled oscillator VCO.

The PLL based industry and trade as the principle of PD is the input signal phase and the VCO output signal phase, than a lose out a positive on the ratio of the two input signal phase difference of electric pressure added to the loop filter lf suppression of noise and high frequency component after add to the VCO control the VCO output frequency of the input signal and the VCO signal phase difference by gradually reduced and finally achieve a dynamic locking.

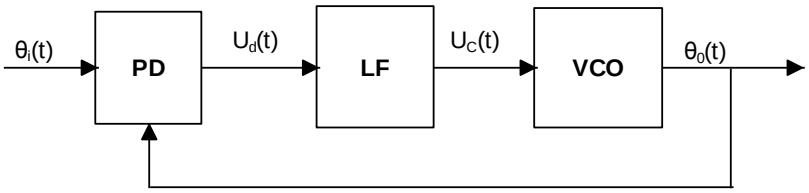

Fig 1.The basic structure of phase locked loop

Phase lock loop in the machine and frequency start stage ring road is out of lock we usually put the ring road into the lock in a process called capture to ensure the ring road must be locked into the natural frequency difference as the trapping band is denoted as to ensure the P Omega loop only phase capture a process called maximal natural frequency difference with L as the rapid capture of Omega in first-order loop only phase trapping in the capture process phase no 2 pi cycle jump ring is of order two we should use most of a Ring Road Ring Road in a total of two integral link so two order loop with phase frequency capture and capture two capture frequency capture the required time called capture time phase capture required When is called fast acquisition time or phase capture time usually frequency capture time is always far greater than phase capture the general said to capture won the capture time is refers to the frequency capture time without considering phase capture ring.

When the ring road in the locked state when the output frequency and input frequency are the same between the two in a steady state phase difference if the input signal occurs phase or frequency of interference or modulation caused by the ring road through self control with the loop output signal, the voltage controlled oscillator frequency and the phase will track the input signal changes this is the tracking characteristics of commonly used input signal form three phase step frequency step and frequency ramp from the input signal changes the transient phase error and steady-state phase error of the small ring road line is a measure of the tracking performance is good to bad sign when it are not only with the ring road itself is also related with the parameters of input signal Relevant form.

The frequency synthesizer has six main performance index of the:1. output frequency of 2 step frequency step 3 frequency drift frequency refers to the long-term stability of the main drift and Shi Piao 4 stray suppression of non harmonic wave and output frequency not to do without using frequency components and the ratio of 5 is the carrier level short term stability of the frequency domain shows it can be regarded as the type of random noise signal of spectrum with frequency modulation from frequency domain to frequency spectrum is no longer a discrete spectrum with a wide band usually used in the distance the heart rate of a single frequency frequency at a bandwidth in the noise energy and the center frequency ratio of the energy to represent 6 hop frequency from one frequency to another frequency when the error rate is small in specified frequency Time used for value.

3. Low phase noise analysis of the phase locked loop

In radio communication and radar technology in system sensitivity and selectivity is a difficult point of design and key points in front the main limitation is due to the number of noise index and non line organ pieces but with low noise device improvement the dynamic range of the expansion of the system and improve the gain of these questions is to solve now by radio communication and radar technology to improve the system of higher and more strict requirements for the new limiting factors what caused from this aspect the work of science and technology personnel's attention and research of the new main limiting factors of phase noise is more like a sideband noise that is visible to the research of phase locked loop Research on the phase noise index is especially important.

Lock phase loop frequency synthesis is main by the frequency doubling device put high frequency divider mixed discriminator phase voltage controlled oscillator is the circuit group into which also includes auxiliary collector circuit of frequency hopping control circuit and an electronic switch, etc. they are not with degree of introducing noise to frequency synthesizer, so the noise of the frequency synthesizer components is necessary.

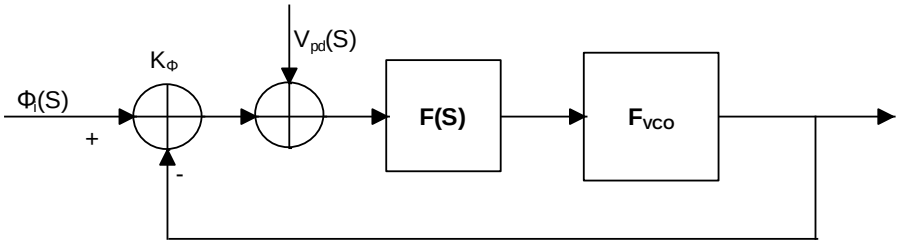

Fig 2.Considering phase detector leakage PLL

In the phase lock loop with variable except N frequency divider can be to solve two key problems is first without changing the input reference frequency can change the VCO output frequency for the actual should be used provided convenient followed by increase the output frequency resolution reduces the reference frequency of the phase discriminator.

The front section of the reference crystal oscillator to the outer ring road in a phase locked loop in the noise of this section from the system level to discuss the phase locked loop phase noise distribution group discussion of each noise source on the ring road noise contribution and a total of PLL and the phase noise spectrum of noise and interference with random body analysis is very difficult though we can use as the AGINENT ADS simulation software and MATHCAD and other large calculation software one for analysis but we must have the aid of PLL linear phase model began to research.

In addition to the influence of phase noise due to the number to a more it will also affect the phase factor Noise indicators in the following also to make a simple note:

1 VCO of band noise contribution in front for the estimation of phase noise in VCO in band noise influence is omitted from figure 37 but not see the fact of VCO band is a noise is influential in the VCO ring in noise the acoustic transfer function is increasing and the VCO phase noise function curve is decreasing when the two letter number by the result when the flat so that the VCO noise will be superimposed to the band noise on the road to a very narrow band width when the loop or VCO noise

when the sound is VCO in the loop bandwidth on the phase noise of the impact will be greater this behind me in the narrow band PLL frequency synthesizer design will see.

The 2 charge pump current on the phase noise index of the influence of the multi frequency synthesizer chip is programmable to set type charge pump current which is through adjusting the charge pump current to improve the phase noise index can be provided from the transfer function the number of the charge pump noise is charge pump current gain phase except but usually when the charge pump current increases when the charge pump noise will increase but in some situations when the charge pump with current phase noise has no area don't but in another case of a charge pump with high current phase noise is better if the United States National Semi-conductor Corporation LMX23x series when the charge pump current from 4m A to 1m A phase noise index of 4D B and the evil, when electricity Charge pump current low to 1m a electric charge pump flow on phase noise refers to the influence is very small charge pump gain on the phase noise influence and specific PLL chip related

3 double phase lock loop chip used in dual phase lock loop chip in when the core of a ring road another ring road although received the VCO, but in power saving mode to obtain a better phase noise index of this kind of situation than two ring road at the same time in a 2 D B phase noise improvement such as if the two ring road with enable and when two PLL output frequency is near the phase noise degradation will be more serious

4 phase noise refers to the standard of reference crystal oscillator considered although front false design of a charge pump noise and kill the frequency rate of synthesis for phase noise such as fruit reference crystal oscillator noise is poor the situation may have different crystal vibration noise is not in phase noise level accounted for the dominant position of a method is the crystal oscillator frequency rate twice frequency with the R value becomes twice the original if phase noise change which shows the oscillator noise dominates the.

4. The principle and the application of a number of lock phase ring

The characteristics of the whole number of points than the frequency phase locked loop frequency synthesis device is when each programmable program consists of frequency ratio changes (increase or decrease) to the output frequency of the change amount of the reference frequency FR in order to improve the frequency resolution will be to reduce the reference frequency fr the result caused by the transfer time extension which is a pair of contradictory points number of phase lock loop (Fraction-N PLL) can solve this contradiction points the number of phase locked loop as early as 20 years ago began its research but until recently only a few years to full attention score _N technology is abroad 70 years beginning in swallow spit pulse technology on the basis of the research work when called digital phase after Racal HP is called F-N is now in a foreign country in a good solution The frequency synthesis device and it should be with frequency synthesis technology equipment has universal used this technique to score _N points frequency phase locked loop frequency synthesis of the frequency ratio is a small number of N F in the N is the entire frequency ratio the number of F is the decimal part of the frequency ratio in frequency than the minimum variable is less than 1 so that it can not change the reference frequency of FR under the condition of high frequency resolution if the frequency resolution to keep swallowing lock count the phase loop resolution can improve the reference frequency of FR from the system transfer time is shortened at the same time through the high frequency phase can increase the loop bandwidth and strong feedback is more of the same to the frequency Step into the next by to N, the number of lock phase ring can take great learning phase this frequency at the same frequency output can lower integer n, in down low and integer n related parameters test phase noise multiplying the evil of from and can be obtained more good than the NPLL ring road noise performance is provided for the high frequency spectrum purity and price ratio can be said to the frequency synthesis device technology breakthrough below will work principle of Fractional-N PLL as a brief introduction.

The FNPLL fraction _N ring road work principle of NPLL ring road has great improvement though it is very similar to the NPLL ring road work in addition to a new increase in several parts of the F register and method for phase accumulator and pulse to remove and die quasi phase interpolator API, including

D/A converter inverter and it includes all the components of the FNPLL NPLL loop loop start work first need to divide the number of F in the form of BCD code stored in the number of registers through the microprocessor. The reason is then in each reference period the fractional part with the phase accumulator and method for content in addition and return to the phase accumulator of this kind in any moment of the phase accumulator in the general store At that time, the amount of VCO weeks of the previous period of ultra.

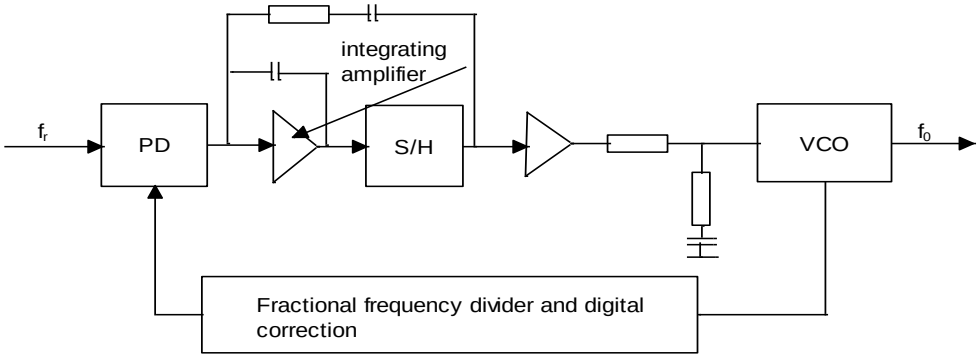

Fig 3.Principle block diagram of FNPLL frequency synthesizer with digital correction

5. Design of three - order non - source filter

Third order non source Ring Road filter wave device is on the basis of second order non source filter with a low pass filter to further suppression of stray combined chart a third-order non source ring.

A source of loop filter in phase locked loop design is often used to it, and to adopt before the loop charge pump power source is similar to the ring road will lead into a source device using a source of noise but the loop filter is has its advantages: it allows the charge pump output voltage bias to the charge pump power source voltage of a half the sample, the charge pump can get better matching, which can reduce the charge pump mismatch in the stray has two kinds of forms are ring road electric source filter topology node in common structure which is the two ring road output can reach the power source voltage operational amplifier with high frequency control voltage output of two ring road form than they have Advantages of the a ring road and its circuit structure is simple, such as figure 3A 5 the second ring road is it and before electric pressure type electric charge pump structure is more similar to it very familiar, loop electric capacity is more reasonable.

Knot theory: two have source loop topology structure of the operational amplifier bias in the charge pump power supply pressure of the center point and to reduce the stray with by to make with the transport increased the isolation which allow reduces the VCO input electric capacity and loop filter filter noise impact the also is two of the structure of the filter and the.

On the surface of said low noise phase lock design scheme and method in low phase noise phase locked loop plays for different design requirements with the selected design scheme is not the same as the design frequency step is 1KHz under low noise jump you can't choose the frequency source with the number of _N phase lock frequency source if the frequency step less the number of stray more dense it will lift high frequency source phase noise from the frequency spectrum instrument on the outside we should also note the number of points at _N the number of divider in general of 1215 to DDS, we should note its output frequency is limited here we selected multi ring scheme that can meet the low frequency resolution and can achieve the phase of high phase Noise that marked in some specific design needs the multiple design case and the method fully synthetic should be used to ensure lock phase jump frequency source it the refers to the greater design and debugging of the space to improve the phase noise indicators have reached the low phase noise design objective.

6. A case of low noise phase locked loop

Low noise lock phase ring design involves all aspects of surface technology to ask questions which package including system design case extraction with body circuit design circuit of a printed board

layout and etc. each ring section of jumping frequency source of phase noise and it refers to standard has very big influence under the class, I do some low noise lock phase jump frequency source with body design to discuss the low noise phase locked frequency hopping source low noise design.

Double frequency converter tube connecting a frequency doubling the frequency doubling chain structure complex debugging difficult step to restore the two transistor can resolve the problem of high frequency doubling time of single step recovery diode can be two to ten times or even several hundred times double frequency step recovery diode two in micro wave small power source comb wave generator sampling oscilloscope was to be widely used for the convenience of discussion under the uniform step recovery diode for short step tube step recovery diode S R D two SRD is an ideal nonlinear element is a PN junction diode two plus positive voltage when it and the PN junction two pole tube like positive conduction but when the external voltage from positive to become negative after And are suitable in the double turn step tube and not horses cut to and there is a very large reverse current flow to a minute at a very fast speed to cut to the state to form a current pulse step and the element in a very high impedance near the road is that it is a very good state impedance electronic switch element harmonic wave produced principle is based on the impedance change dependent charge as a function when the sine wave excitation in each cycle can produce a very narrow pulse impulse harmonic rich and high efficiency.

Modern communication and radar technology of frequency source index requirements more and more high especially the phase noise, it has become a system about modern power system in a bottle neck for the number of phase locked loop for each part of the ring road noise. Offer hand ring road noise distribution of a frequency spectrum can be obtained by the low noise phase locked loop design of the related theory and proposed a more accurate prediction algorithm. For some low noise design scheme. The Xi Wen chapter gives me the three low noise phase locked frequency source design with mixed PLL frequency hopping source with narrow frequency and phase locked source N phase lock frequency source are obtained very good Phase noise index although I in this subject obtained the certain achievement but in the fields is not enough road in on side by in time have some problem analysis is difficult to avoid will have the deficient in the design surface due to the water level and the check for will be hard to avoid has not enough place again and into release bin promote on the error in the hard to avoid also hope the expertsA professor of criticism.

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