Design of an Improved Algorithm for Target Tracking System

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Abstract

This paper designed a real- time system of video image processing based on TI DSP of TMS320C6472 and Altera FPGA of EP3C25E144C8N.The original data are firstly filtered using median filter with 3x3 windows, then, transmitted to DSP by Ping-Pang method.The histogram is selected as the object characteristic, and is compared with histogram projection for object tracking. The fixed pointer operation is used for fast computing velocity, instead of the floating pointer operation.The experiment results show that hardware architecture is effective and feasible, the performance meets the requirement of real- time processing, and the system has a significant practical application value.

Keywords

Terms-Real-time tracking;Median filter;Histogram projection; Ping- pong operation;

1. Introduction

Television image tracking is an important research topic in the computer Vision. There are a wide application such as monitoring, video code and the field of military industry. Especially in the active vision system, tracking process can not only obtained a target trajectory of quickly and accurately, but also need to control the tracking turntable, Maintain the target in center of the viewing field, therefore realize the target tracking of continuously[1]. Histogram is the most commonly used to describe arithmetic operators to non-parametric image target, it is simple, easy to express, so it has been widely applications in image processing [2]. Histogram back-projection is a measurement method for description histogram similarity. It is originally advanced as color histogram similarity, which describe image target easily, less count and memory, easily achieve in the Embedded System [3].

Because television image tracking device needs to processing data for field (20ms) or frame（40ms）by frame-by-deal, and also required higher real-time. Therefore, Altera FPGA of EP3C25E144C8N is used as image filter in the system, and realizing hardware fast median filter to tracking data, improve the filter velocity; finally, TI DSP of TMS320C6472 is used as the data core processor, and realized tracking arithmetic of main target.

2. System hardware block diagram and working principle

DSP is used to the core processor of the system, FPGA is used to input pre-processing of forward-channel, CPLD is used to output control of back-channel, its block diagram shown in Fig.1. The system consists of three functional modules which is image acquisition and pre-processing module, the core processing module of DSP, output superimposition module [4-5].

2.1 Image Acquisition and Pre-processing

The model includes SAA7111A as analogy video decoder digital chip[6], FPGA-EP3C25E144C8N as image pre-processing, and RAM1, RAM2 and so on. At work, CCD output a COMPOUND-VIDEO,

which is decoded and digital by video decoder chip, and output Videos synchronous control signals and digital image data; FPGA internal logic according to video control signals, finished the filter processing with input video, and filtered the data is saved to RAM1 or RAM2 according to ping-pang operate logic.

Table1 3×3 Window pixel array

Line	No. 0	No. 1	No. 2
line 0	q0	q1	q2
line 1	q3	q4	q5
line 2	q6	q7	q8

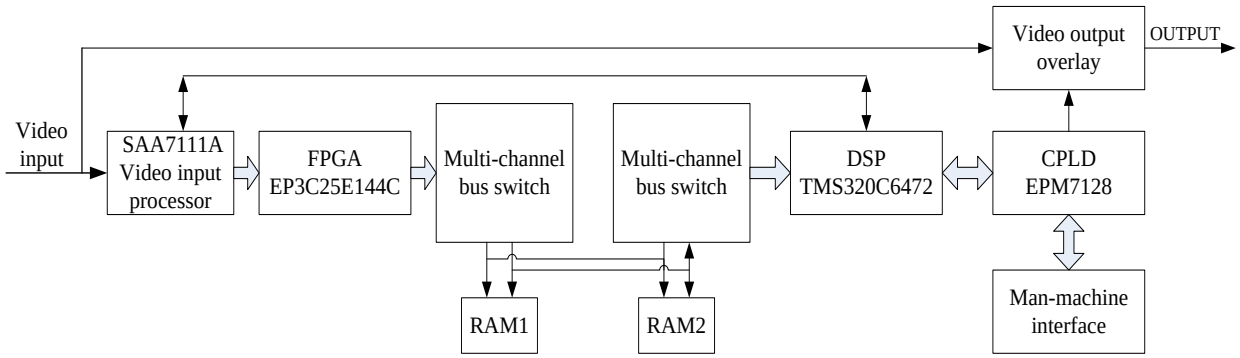


Fig.1Tracking system block diagram

Because of the noise will generate interference to the calculation of the histogram, so should eliminated noise before calculating the histogram. Median filter can filter out noise, and can better protect the edge of the target image characteristics, which is widely used as a means of image pre-processing in engineering. In order to enhance system real-time, the system is realized the fast median filter algorithm using FPGA. The processor is as follows:

Each pixel is defined as q0, q1, q2, q3, q4, q5, q6, q7, q8 in 3 × 3 window, pixel array as shown in table 1:

Filtering process is divided into three steps: first, each column in window should be calculated the Maximum, median and minimum in window. This will be three group data, namely the Maximum group, the median group and the minimum group. Calculation processor as follows:

Maximum group: Max0 = maxq0, q3, q6, Max1 =maxp1, q4, q7, Max2 = maxp2, q5, q8.

Median group : Med0 = medq0, q3, q6, Med1 = medq1, q4, q7, Med2 = medq2, q5, q8.

Minimum group: Min0 = minq0, q3, q6, Min1 = minq1, q4, q7, Min2 = minq2, q5, q8.

In the formula,Max express maximum operation, med express Medium value operation, min express minimum operation. Followed to obtain the following values:

Min_{max} = min [Max_0 , Max_1 ,Max_2]

Med_{med} = med [Med_0 ,Med_1 ,Med_2]

Max_{min} = max [Min_0 ,Min_1 ,Min_2]

Finally obtain a middle value of the above three values, namely:

Winmed = med [Min_{max} , Med_{med} , Max_{min}]

Winmed is medium data of final output. Using this method to calculated for Medium value, which requires comparison for 17 times, compared with the traditional algorithm the number to compare decreased by almost 2 times, and each computing is fully parallel for every step, Its flow chart is as follows:

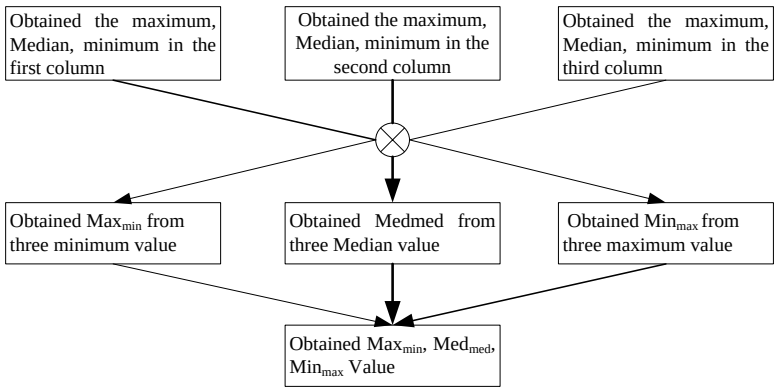


Fig.2 Median filter flow chart

Finally the median filter is generated top-level diagram as follows (Fig.3).

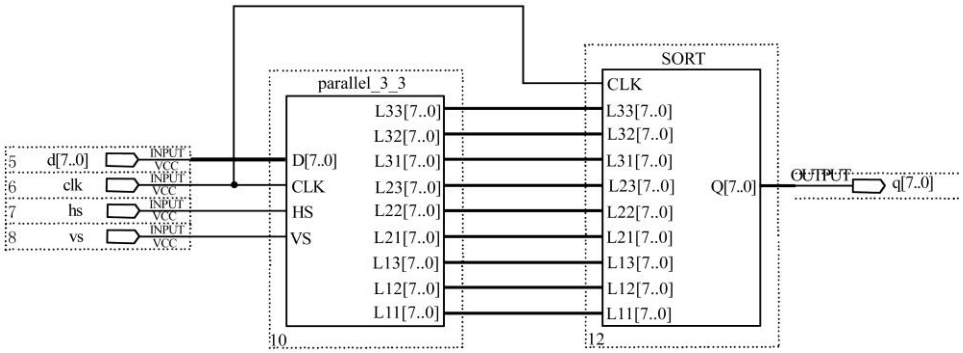


Fig.3 Median filter top-level diagram

Here, parallel_3_3 module is completed serial input image data for the Table1, SORT module completed median filter operation.

2.2 Output Overlay Module

The final output of the system is a composite video image with tracking the results, in the image,it is not only necessary to give target tracking window size, location, but also give target tracking status, target location,tracking time and other related language prompts. Using the character chip UPD6453 as logic output characters dot-matrix of the system[7]; Compiles the window and production logic in the CPLD, and producing tracking window's shape and position; Finally, it is superimposed to the analog video of input through multi-channel analog video MAX4158 chip.UPD6453 is the special characters overlay chip which is Japan's NEC Corporation product, its characteristics are powerful with display editing function, and each character is in a 12 ×18 dot-matrix, both the character size and the flickering frequency may adjust accordance with required;built-in SPI interface can communicates with the microprocessor directly, programming is simple[6]. Fig.4 is the circuit diagram of uPD6453 and overlay circuit.

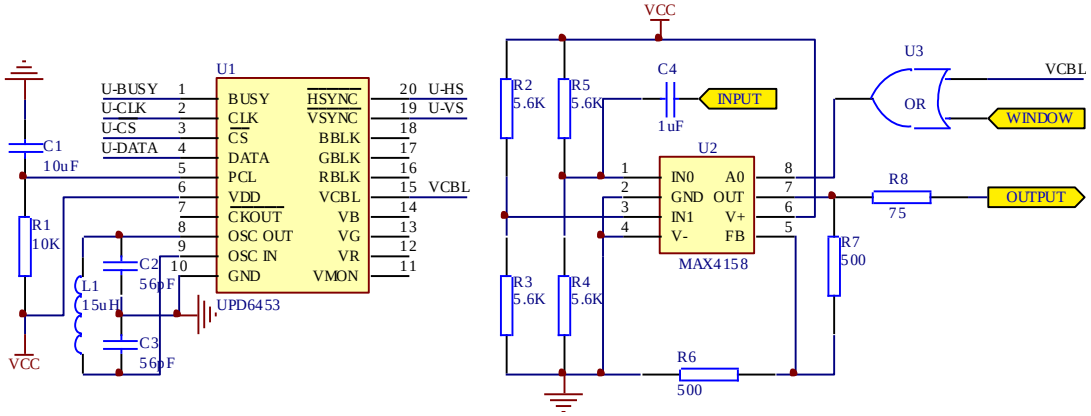


Fig.4 Overlay module circuit diagram of character and window

TMS320C6472 has not integrated SPI interface, here, HPI is configured as general-purpose I/O port for analog communications between SPI and μPD6453, and command of display character will be sent; μPD6453 according to command of input and video lines, field synchronization signals, character overlay dot-matrix logic VCBL that is generated. The characters logical of output and window logic signal WINDOW that CPLD generates takes OR logic, it control max4158 to realize the character superimposition.

2.3 Algorithm Processing Module

Algorithm processing module is consisted of DSP-TMS320C6472, it adopted improved Harvard Bus Structure, and operational capability may achieve 4000MPIS, with three Multi-channel buffered serial interface (MCBSP) and a host port interface (HPI) that can be configured as general purpose I/O pins, and has 8Mbit integrated large-capacity SRAM in the chip. It is a high-performance, low-cost, low-power fixed-point digital signal processor [8-11]. Specific work flow is as follows: after the system started, DSP for user program will loaded onto the internal program space from external FLASH, boot-load successfully started, user program begin to execution. First, program has been initialized for input module SAA7111A, output character module μPD6453, window logic module CPLD, employ their normal job, waiting for sampling and achieve interruption of signal. Once DSP has detected interruption happened, it executes interruption service program. In the interrupt service program,the first reading deal with the external man-machine interface circuit data that detected whether the control command, and makes corresponding processing; On the other hand, reading the input image data from the input image buffer, according to the tracking algorithm, to obtained target's miss distance in the current image, then, calculated results are sent to the output overlay module and output display.

3. Target-tracing algorithm based on back-projection

The histogram back-projection is an express method for histogram feature vector similarity, and used in target tracking, Assuming $M=\{M_i\}$ and $I=\{I_i\}$ are normalization histogram for the target template and matched images, i is a quantized gray value, then ratio histogram is defined as:

$$R_i = \min\left(M_i / I_i, 1\right) \tag{1}$$

Ratio histogram will be mapped into the original image, value of corresponding ratio histogram replace the original image's pixel, and formed histogram back-projection, Structuring the target shape template $D^r_{x,y}$,

$$D^r_{x,y} = \begin{cases} 1, if\left(\sqrt{x^2+y^2}<r\right) \\ 0, \text{ otherwise} \end{cases} \tag{2}$$

Where:(x,y)is location as the target pixel, r is the radius of circum-circle as the object. We choice this template and using it make convolution processing to histogram back-projection, the convolution image peak-value is the corresponding match target location. Tracking calculation steps are as follows:

①Computation object normalization histogram M and according to ② computation corresponding object shape template;

②reading image data of match, computation normalization histogram of image *I*;

③According to ① computation ratio histogram R_i ;

④Corresponding to each pixel, calculated its histogram back-projection, $G=\{g(x,y)\}$, $g(x,y)=R_{h(x,y)}$.

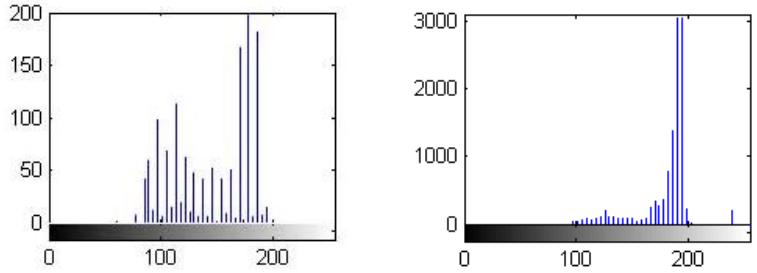
Where: $h(x,y)$ is (x,y) gray value, $g(x,y)$ is gray value for corresponding projection;

⑤Calculated convolution diagram;

⑥Calculated peak of convolution diagram, namely matching the target location and output; Jump to ②.

Fig.5 is a part of tracking the results as a tracking, Fig. 5(a) is tracking window object as the initialization selection, calculates histogram for Fig.5 (d). At tracking frame 38, we give out the histogram of input image for Fig.5(e), back ③~⑤ step, obtained convolution Fig.5(c), in which the bright spot is convolution biggest place that is the object current position.

(a) Original target image; (b) the 38th tracking image; (c) Back-projection convolution diagram



(d) Fig. (a) Histogram diagram; (e) Fig. (b) Histogram diagram

Fig.5 Tracking result demonstration diagram

4. Experimental result

For easy calculation in the experiments,, we select rectangular shape for the target shape template, namely:

$$D_{x,y}^{r}=\begin{cases}1\,,\ if\ \ (abs(x)<r \parallel abs(y)<r)\\ 0\,,otherwise\end{cases} \tag{3}$$

When calculates the ratio histogram, the ratio histogram from (0, 1) between decimal enlarges to (0, 255) the integer, therefore,the fixed pointer operation is instead of the floating pointer operation for fast computing velocity. Here is select 512*256 pixels of image the centre as an effective tracking data, each field calculated a track result, when the target is less than 160 * 80 = 12800 pixels, the algorithm can run in real-time , effective tracking object.

Acknowledgment

This article discussed an approach based on back-projection method to the gray target tracking system's realization. The histogram is selected as the object characteristic, and is compared with histogram back-projection for object tracking. In order to ensure real-time of system, and reduced the calculated amount of each field tracking, in guarantee the accuracy, we are choice the fixed-point operation for fast computing speed. The result of the experiments has shown that the tracking system is real-time and robust.

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